SGX-Step: An Open-Source Framework for Precise Dissection and Practical Exploitation of Intel SGX Enclaves

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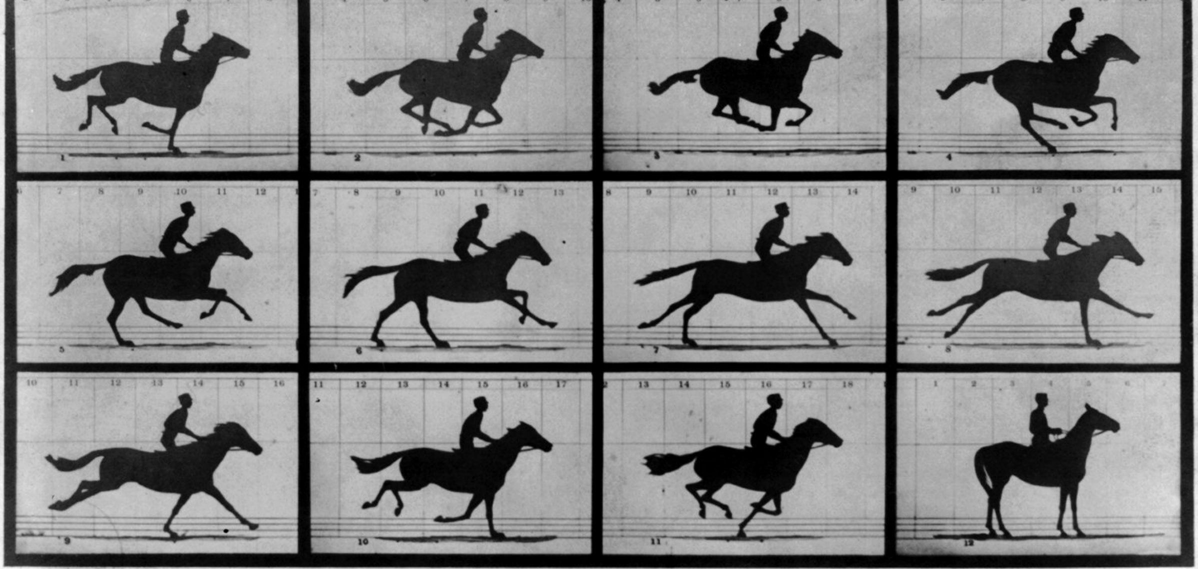
DistriNet
KU LEUVEN

DALL·E 3



MORSE'S Gallery, 417 Montgomery St., San Francisco.

THE HORSE IN MOTION.

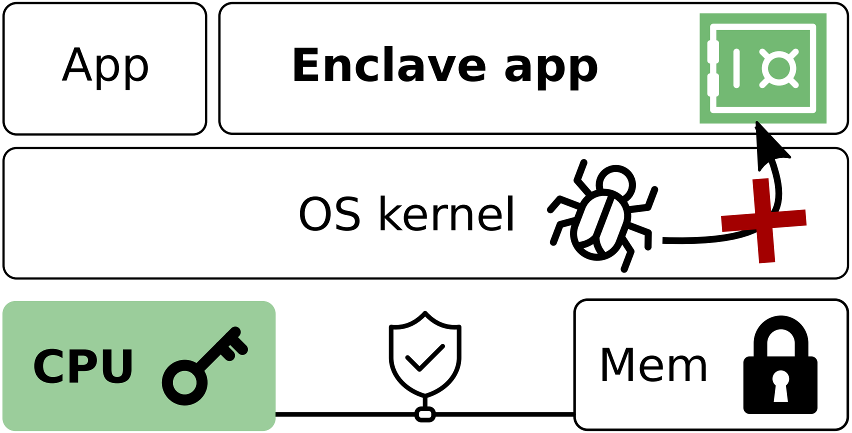
Illustrated by

MUYBRIDGE.

AUTOMATIC ELECTRO-PHOTOGRAPH.

"SALLIE GARDNER," owned by LELAND STANFORD; running at a 1.40 gait over the Palo Alto track, 19th June, 1878.

From Horses to Enclaves: Reducing Attack Surface



Intel SGX promise: Hardware-level **isolation and attestation**

From Horses to Enclaves: Reducing Attack Surface

Game changer: Untrusted OS → new class of powerful **side channels!**

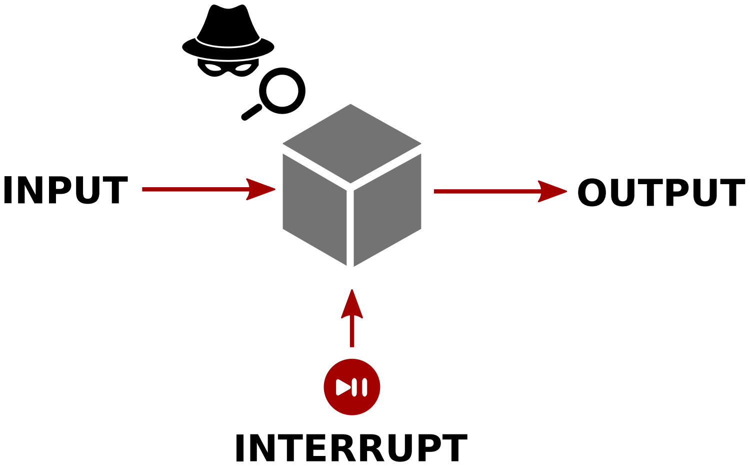
Challenge: Side-channel Sampling Rate

Slow
shutter speed

Medium
shutter speed

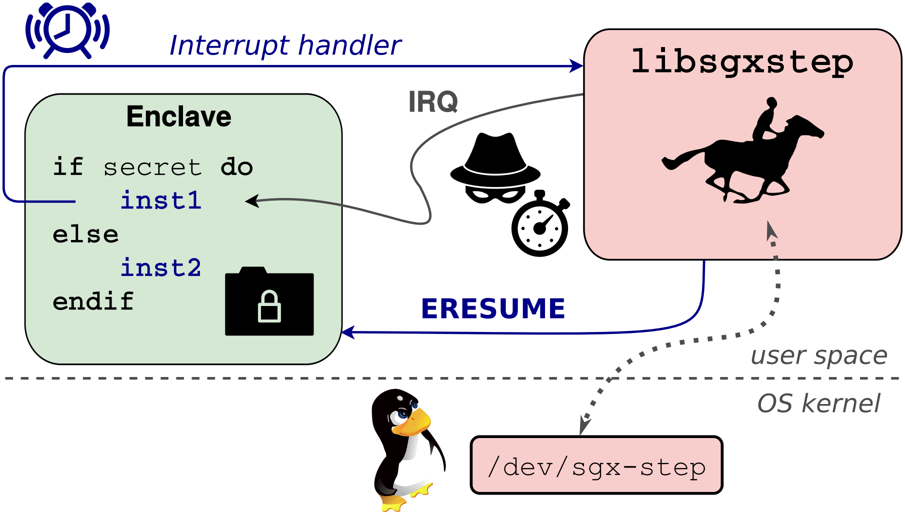
Fast
shutter speed

SGX-Step: Executing Enclaves one Instruction at a Time



🗋 Van Bulck et al., "SGX-Step: A Practical Attack Framework for Precise Enclave Execution Control", SysTEX 2017.

SGX-Step: Executing Enclaves one Instruction at a Time



Van Bulck et al., "SGX-Step: A Practical Attack Framework for Precise Enclave Execution Control", SysTEX 2017.

A Retrospective of 5 Years of SGX-Step Development

SGX-Step

https://github.com/jovanbulck/sgx-step

Unwatch 27 | Fork 82 | Star 402

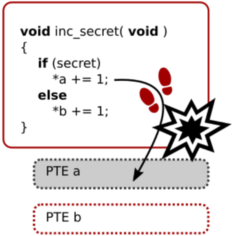
- Became **de-facto standard** for interrupt-driven attacks
- Actively maintained & supported
- Widely recognized:
  - > 400 GitHub stars
  - > 215 academic citations
- Marked influence on both **attacks & defenses** on SGX and beyond

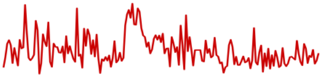
Highlight #1: Impact on Attacks

SGX-Step: Enabling a New Line of High-Resolution Attacks

Yr	Venue	Paper	Step	Use Case	Drv
'15	S&P	Ctrl channel [XCP15]	~ Page	*Probe* (page fault)	✓
'16	ESORICS	AsyncShock [WKPK16]	~ Page	*Exploit* (mem safety)	–
'17	CHES	CacheZoom [MIE17]	✗ >1	*Probe* (L1 cache)	✓
'17	ATC	Hahnel et al. [HCP17]	✗ 0 - >1	*Probe* (L1 cache)	✓
'17	USENIX	BranchShadow [LSG+17]	✗ 5 - 50	*Probe* (BPU)	✗
'17	USENIX	Stealthy PTE [VBWK+17]	~ Page	*Probe* (page table)	✓
'17	USENIX	DarkROP [LJJ+17]	~ Page	*Exploit* (mem safety)	✓
'17	SysTEX	SGX-Step [VBPS17]	✓ 0 - 1	*Framework*	✓
'18	ESSoS	Off-limits [GVBPS18]	✓ 0 - 1	*Probe* (segmentation)	✓
'18	AsiaCCS	Single-trace RSA [WSB18]	~ Page	*Probe* (page fault)	✓
'18	USENIX	Foreshadow [VBMW+18]	✓ 0 - 1	*Probe* (transient exec)	✓
'18	EuroS&P	SgxPectre [CCX+19]	~ Page	*Exploit* (transient)	✓
'18	CHES	CacheQuote [DDME+18]	✗ >1	*Probe* (L1 cache)	✓
'18	ICCD	SGXlinger [HZDL18]	✗ >1	*Probe* (IRQ latency)	✗
'18	CCS	Nemesis [VBPS18]	✓ 1	*Probe* (IRQ latency)	✓
'19	USENIX	Spoiler [IMB+19]	✓ 1	*Probe* (IRQ latency)	✓
'19	CCS	ZombieLoad [SLM+19]	✓ 0 - 1	*Probe* (transient exec)	✓
'19	CCS	Fallout [CGG+19]	–	*Probe* (transient exec)	✓
'19	CCS	Tale of 2 worlds [VBOM+19]	✓ 1	*Exploit* (mem safety)	✓
'19	ISCA	MicroScope [SYG+19]	~ 0 - Page	*Framework*	✗
'20	CHES	Bluethunder [HMW+20]	✓ 1	*Probe* (BPU)	✓
'20	USENIX	Big troubles [WSBS19]	~ Page	*Probe* (page fault)	✓
'20	S&P	Plundervolt [MOG+20]	–	*Exploit* (undervolt)	✓
'20	CHES	Viral primitive [AB20]	✓ 1	*Probe* (IRQ count)	✓
'20	USENIX	CopyCat [MVBH+20]	✓ 1	*Probe* (IRQ count)	✓
'20	S&P	LVI [VBMS+20]	✓ 1	*Exploit* (transient)	✓
'20	CHES	A to Z [AGB20]	~ Page	*Probe* (page fault)	✓
'20	CCS	Déjà Vu NSS [uHGDL+20]	~ Page	*Probe* (page fault)	✓
'20	MICRO	PTHammer [ZCL+20]	–	*Probe* (page walk)	✓
'21	USENIX	Frontal [PSHC21]	✓ 1	*Probe* (IRQ latency)	✓
'21	S&P	CrossTalk [RMR+21]	✓ 1	*Probe* (transient exec)	✓
'21	CHES	Online template [AB21]	✓ 1	*Probe* (IRQ count)	✓
'21	NDSS	SpeechMiner [XZT20]	–	*Framework*	✓
'21	S&P	Platypus [LKO+21]	✓ 0 - 1	*Probe* (voltage)	✓
'21	DIMVA	Aion [HXCL21]	✓ 1	*Probe* (cache)	✓
'21	CCS	SmashEx [CYS+21]	✓ 1	*Exploit* (mem safety)	✓
'21	CCS	Util::Lookup [SBWE21]	✓ 1	*Probe* (L3 cache)	✓
'22	USENIX	Rapid prototyping [ESSG22]	✓ 1	*Framework*	✓
'22	CT-RSA	Kalyna expansion [CGYZ22]	✓ 1	*Probe* (L3 cache)	✓
'22	SEED	Enclyzer [ZXTZ22]	–	*Framework*	✓
'22	NordSec	Self-monitoring [LBA22]	~ Page	*Defense* (detect)	✓
'22	AutoSec	Robotic vehicles [LS22]	✓ 1 - >1	*Exploit* (timestamp)	✓
'22	ACSAC	MoLE [LWM+22]	✓ 1	*Defense* (randomize)	✓
'22	USENIX	AEPIC [BKS+22]	✓ 1	*Probe* (I/O device)	✓
'22	arXiv	Confidential code [PSL+22]	✓ 1	*Probe* (IRQ latency)	✓
'23	ComSec	FaultMorse [HZL+23]	~ Page	*Probe* (page fault)	✓
'23	CHES	HQC timing [HSC+23]	✓ 1	*Probe* (L3 cache)	✓
'23	ISCA	Belong to us [YJF23]	✓ 1	*Probe* (BPU)	✓
'23	USENIX	BunnyHop [ZTO+23]	✓ 1	*Probe* (BPU)	✓
'23	USENIX	DownFall [Mog23]	✓ 0 - 1	*Probe* (transient exec)	✓
'23	USENIX	AEX-Notify [CVBC+23]	✓ 1	*Defense* (prefetch)	✓

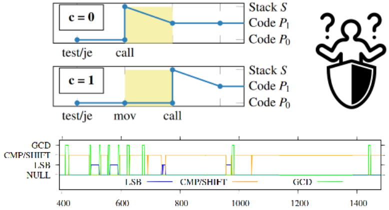
A Versatile Open-Source Attack Toolkit





Interrupt latency

[CCS'18, USENIX'21]



Page-table manipulation

[AsiaCCS'18, USENIX'18-23, CCS20, CHES'20, NDSS'21]

SGX-Step

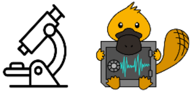
Interrupt counting

[CCS'19, CHES'20-21, USENIX'20]

High-resolution probing

[CCS'19/21, CHES'20, S&P'20-21, USENIX'17/18/22]

[USENIX'18, CCS'19, S&P'21] **Zero-step replaying**



SGX-Step demo: Building a `memcmp()` Password Oracle

```
[idt.c] DTR.base=0xfffffe0000000000/size=4095 (256 entries)
[idt.c] established user space IDT mapping at 0x7f7ff8e9a000
[idt.c] installed asm IRQ handler at 10:0x56312d19b000
[idt.c] IDT[ 45] @0x7f7ff8e9a2d0 = 0x56312d19b000 (seg sel 0x10); p=1; dpl=3; type=14; ist=0
[file.c] reading buffer from '/dev/cpu/1/msr' (size=8)
[apic.c] established local memory mapping for APIC_BASE=0xfee00000 at 0x7f7ff8e99000
[apic.c] APIC_ID=2000000; LVTT=400ec; TDCR=0
[apic.c] APIC timer one-shot mode with division 2 (lvtt=2d/tdcr=0)

--------------------------------------------------------------------------------
[main.c] recovering password length
--------------------------------------------------------------------------------

[attacker] steps=15; guess='******'
[attacker] found pwd len = 6

--------------------------------------------------------------------------------
[main.c] recovering password bytes
--------------------------------------------------------------------------------

[attacker] steps=35; guess='SECRET' --> SUCCESS

[apic.c] Restored APIC_LVTT=400ec/TDCR=0)
[file.c] writing buffer to '/dev/cpu/1/msr' (size=8)
[main.c] all done; counted 2260/2183 IRQs (AEP/IDT)
jo@breuer:~/sgx-step-demo$
```

Highlight #2: Impact on Defenses

Hardening Enclaves against Single-Stepping

SGX-Step sets the **bar for adequate side-channel defenses!**

→ (e.g., LVI, compiler, static analysis, constant-time, etc.)

"ineffective if the attacker can single-step through the enclave using the recent SGX-Step framework. Taking into account these stronger attacker capabilities, we propose a new defense. . . " [HLLP18]

SGX-Step inspired several dedicated **hardware-software mitigations**

→ Collaboration with Intel on AEX-Notify: Innovative hardware-software co-design included in recent processors

→ Probabilistic: SGX-Step remains relevant!

CHAPTER 8
ASYNCHRONOUS ENCLAVE EXIT NOTIFY AND THE EDECCSSA USER LEAF FUNCTION

8.1 INTRODUCTION

Asynchronous Enclave Exit Notify (AEX-Notify) is an extension to Intel® SGX that allows Intel SGX enclaves to be notified after an asynchronous enclave exit (AEX) has occurred. EDECCSSA is a new Intel SGX user leaf function (ENCLU[EDECCSSA]) that can facilitate AEX notification handling, as well as software exception handling. This chapter provides information about changes to the Intel SGX architecture that support AEX-Notify and ENCLU[EDECCSSA].

The following list summarizes the add
details are provided in Section 8.3):

- SECS.ATTRIBUTES.AEXNOTIFY: Th
- TCS.FLAGS.AEXNOTIFY: This enclave thread may receive AEX notifications.
- SSA.GPRSGX.AEXNOTIFY: Enclave-writable byte that allows enclave software to dynamically enable/disable AEX notifications.

An AEX notification is delivered by ENCLU[ERESUME] when the following conditions are met:

SGX-Step led to **new x86 processor instructions!**

→ *shipped in millions of devices ≥ 4th Gen Xeon [CVBC+23]* phoronix

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Intel AEX Notify Support Prepped For Linux To Help Enhance SGX Enclave Security

Written by Michael Larabel in Intel on 6 November 2022 at 06:01 AM EST. 5 Comments

Future Intel CPUs and some existing processors via a microcode update will support a new feature called the Asynchronous EXit (AEX) notification mechanism to help with Software Guard Extensions (SGX) enclave security. Patches for the Linux kernel are pending for implementing this Intel AEX Notify support with capable processors.

Intel's Asynchronous EXit (AEX) notification mechanism lets SGX enclaves run a handler after an AEX event. Those handlers can be used for things like mitigating SGX-Step as an attack framework for precise enclave execution control.

Code 1 in intel/linux-sgx Filter

sdk/trts/linux/trts_mitigation.S

```
 * Description:
 *     The file provides mitigations for SGX-Step
 */
 *  Function:
constant_time_apply_sgxstep_mitigation_and_continue_execution
 *      Mitigate SGX-Step and return to the point at which the
most recent
 *      interrupt/exception occurred.
```

SGX-Step led to **changes in major OSs and enclave SDKs**

Beyond SGX-Step: Derived Frameworks for Emerging TEEs

SGX-Step has inspired similar single-stepping frameworks for alternative TEEs

→ e.g., AMD SEV, intel TDX, arm TrustZone

Independent testimonies on SGX-Step's impact

- *"In the hope that the framework inspires a similar community as SGX-Step, we dubbed it SEV-Step." [WWRE23]*
- *"Leveraging SGX-Step type attack to compromise Intel TDX, which is coined as TDX-Step [. . .] Working exploit well within the timeline but also collaborated closely with the Intel TDX architecture team to review and refine the mitigation for the vulnerability." [Int23]*

Conclusions and Outlook

Paradigm shift: Extremely high-resolution enclave attacks

Hardware-software **mitigations** for new and emerging TEEs

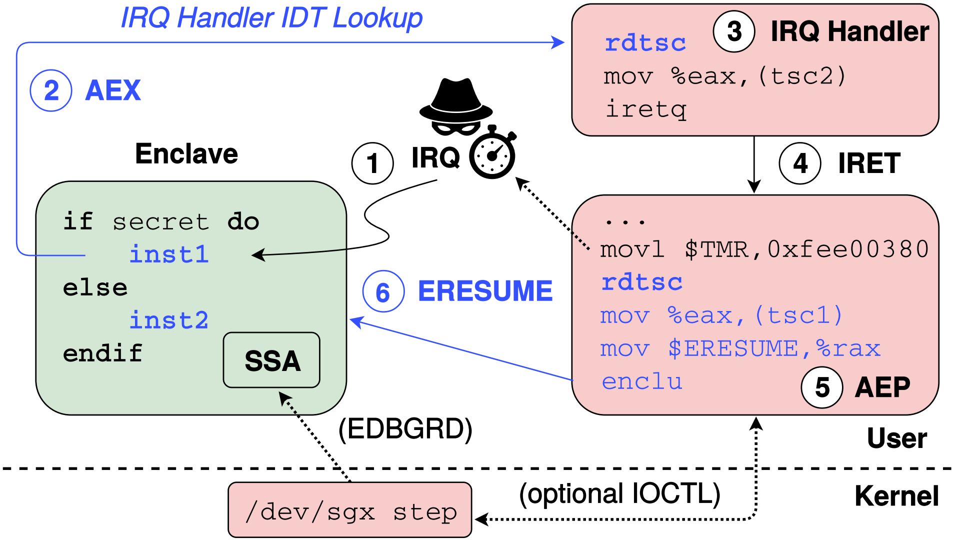
Open-source attack framework sets the bar for defenses!

SGX-Step

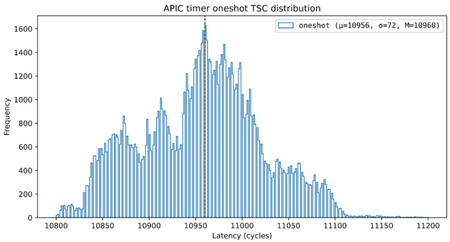
Thank you! Questions?

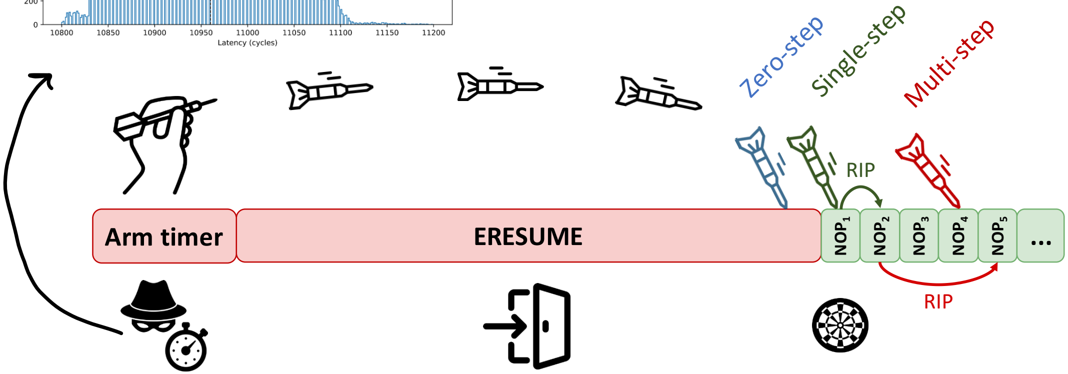
Appendix

Interrupting and Resuming SGX Enclaves



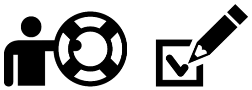
Root-causing SGX-Step: Aiming the timer interrupt

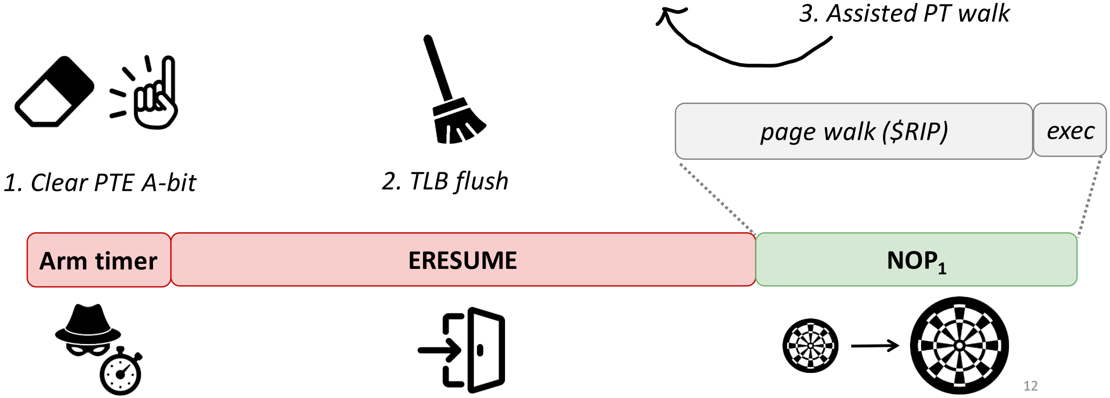




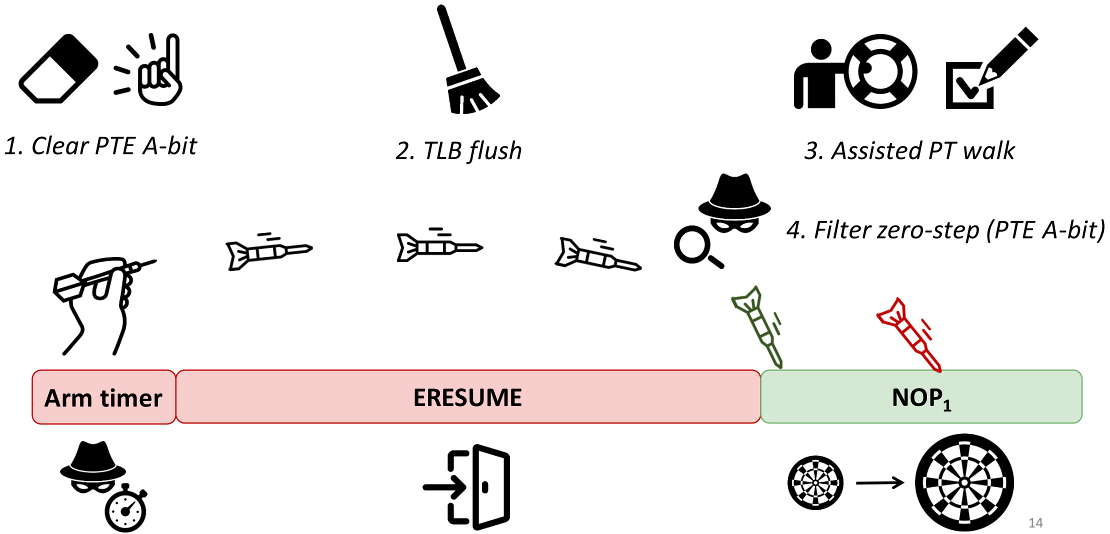
Root-causing SGX-Step: Microcode assists to the rescue!

PTE A-bit	Mean (cycles)	Stddev (cycles)
A=1	27	30
A=0	666	55

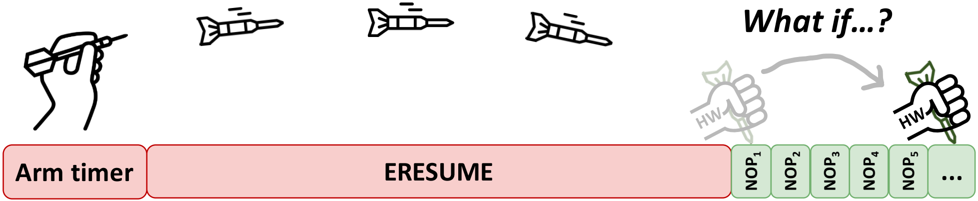


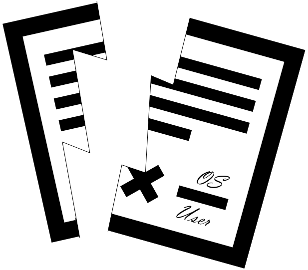


Root-causing SGX-Step: Microcode assists to the rescue!

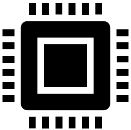


Ideas that were rejected (2)

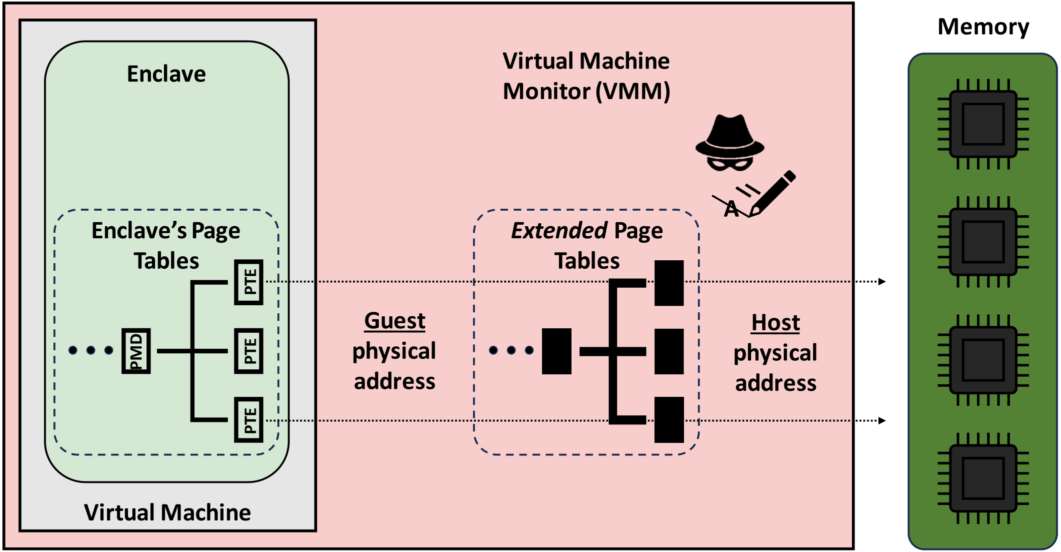




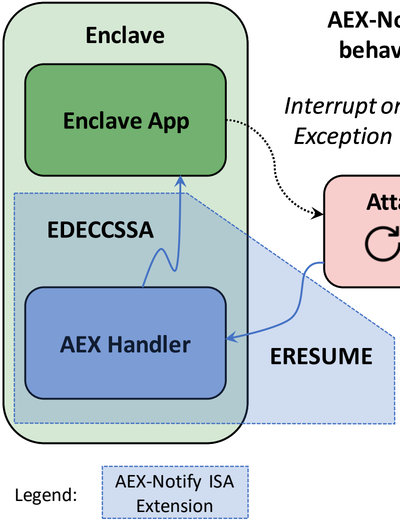
Highly complex

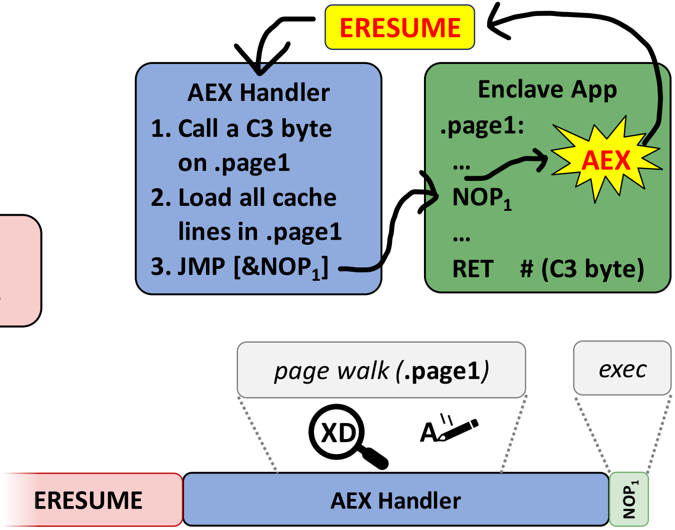


Ideas that were rejected (3)



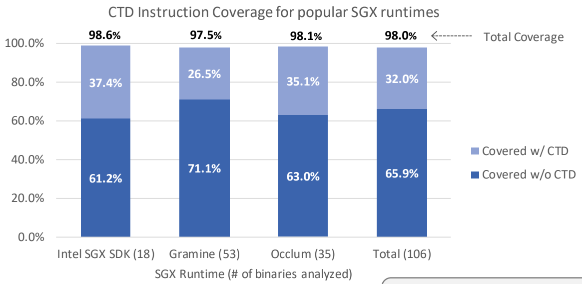
AEX-Notify solution overview

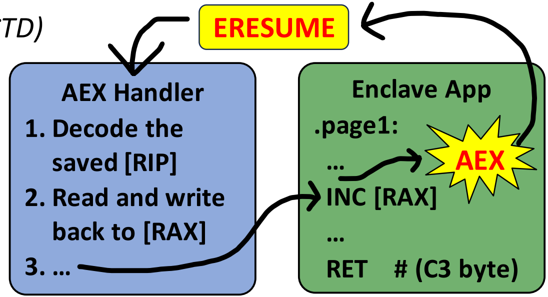


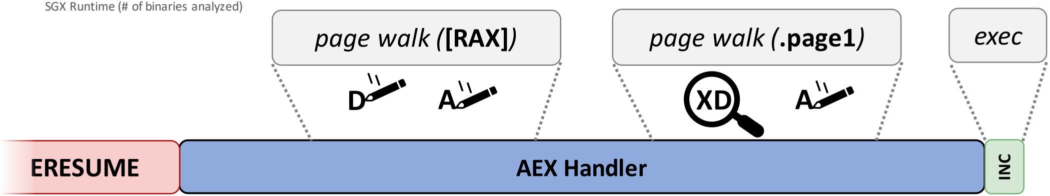


AEX-Notify solution overview

We implemented a fast, constant-time decoder (CTD)







TECHNIQUES AND TECHNOLOGIES TO ADDRESS MALICIOUS SINGLE-STEPPING AND ZERO-STEPPING OF TRUSTED EXECUTION ENVIRONMENTS

TECHNICAL FIELD

[0001] The disclosure relates generally to electronics, and, more specifically, an embodiment of the disclosure relates to techniques and technologies to address malicious single-stepping and zero-stepping of trusted execution environments (TEEs).

BACKGROUND

[0002] Trusted Execution Environments (TEEs), such as Intel® Software Guard Extensions (Intel® SGX), are susceptible to methods that induce interrupts or exceptions to maliciously single-step (e.g. SGX-Step) or zero-step instruction processing in the TEE (e.g. Microscope replay attack, PLATYPUS power side-channel attack). During single-stepping or zero-stepping, a malicious hypervisor or operating system (OS) may be able to increase the granularity of side channel information which can be collected during the TEE processing. Analyzing side channel information is a method that can be used to infer information, such as instruction flows and data, about the TEE. Thus, there is value in techniques that can mitigate these attack techniques, specifically single-stepping and zero-stepping of TEEs.

side-channel attack) and then resumes execution of the code from the enclave according to embodiments of the disclosure.

[0011] FIG. **8** illustrates a method of handling an asynchronous exit of the execution of code from an enclave that utilizes an enclave enter instruction, an enclave exit instruction, and an enclave resume instruction that invokes a handler to handle an operating system signal caused by the asynchronous exit and then resumes execution of the code from the enclave according to embodiments of the disclosure.

[0012] FIG. **9** illustrates a method of handling an exception with an enclave that comprises a field to indicate a set of one or more exceptions to suppress, and when execution of the code in the enclave encounters the exception, a handler is invoked without delivering the exception to an operating system according to embodiments of the disclosure.

[0013] FIG. **10** illustrates a hardware processor coupled to storage that includes one or more enclave instructions (e.g., an enclave resume (ERESUME) instruction) according to embodiments of the disclosure.

[0014] FIG. **11** is a flow diagram illustrating operations of a method for processing an "ERESUME" instruction according to embodiments of the disclosure.

[0015] FIG. **12** is a flow diagram illustrating operations of another method for processing an "ERESUME" instruction according to embodiments of the disclosure.

[0016] FIG. **13**A is a block diagram illustrating a generic

Configuring the Timer Interrupt

🔔 **SGX-Step goal:** Executing enclaves one instruction at a time

Challenge: we need a very precise timer interrupt:

☹ x86 hardware *debug features* disabled in enclave mode

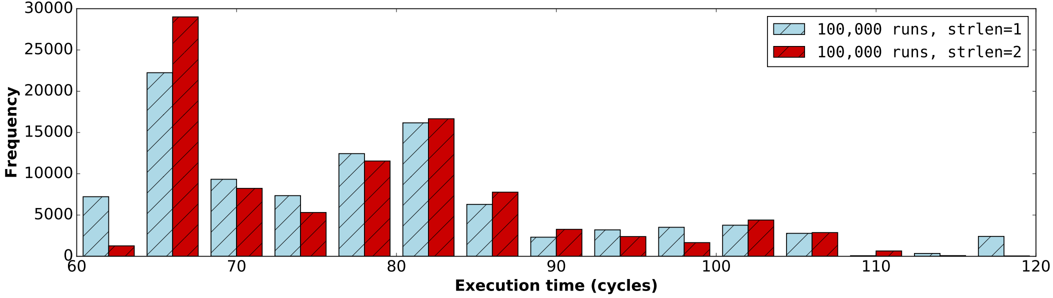
☺ . . . but we have *root access!*

⇒ Setup user-space virtual **memory mappings** for x86 APIC (+ PTEs)

```
jo@sgx-laptop:~$ cat /proc/iomem | grep "Local APIC"
fee00000-fee00fff : Local APIC
jo@sgx-laptop:~$ sudo devmem2 0xFEE00030 h
/dev/mem opened.
Memory mapped at address 0x7f37dc187000.
Value at address 0xFEE00030 (0x7f37dc187030): 0x15
jo@sgx-laptop:~$
```

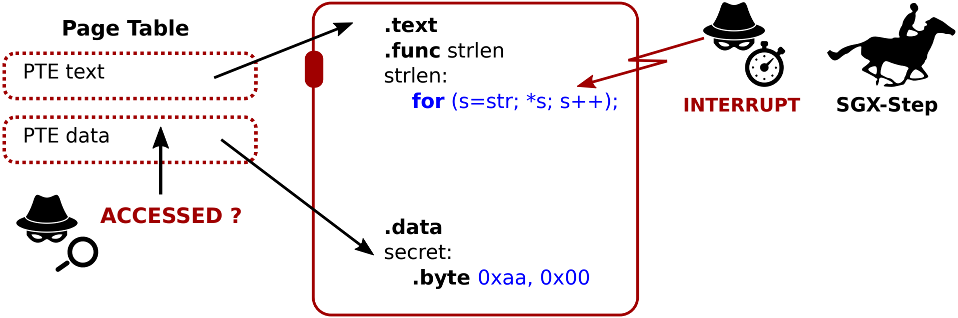
Building the `strlen()` side-channel oracle with execution timing?

Too noisy: modern x86 processors are lightning fast. . .



Counting `strlen()` loop iterations with SGX-Step

Page table accessed bit set? → **strlen++** → resume



Demo: Breaking AES-NI with the `strlen()` null byte oracle

```
Useless leakage 48 for 484
Useless leakage 48 for 485
Useless leakage 48 for 486
Useless leakage 48 for 487
Useless leakage 48 for 488
Useless leakage 48 for 489
Useless leakage 48 for 490
Useless leakage 48 for 491
Useless leakage 48 for 492
Useless leakage 48 for 493
Useless leakage 48 for 494
Useless leakage 48 for 495
Useless leakage 18 for 496
Useless leakage 48 for 497
Useless leakage 48 for 498
Useless leakage 48 for 499
Useless leakage 48 for 500
Useless leakage 48 for 501
Useless leakage 48 for 502
Useless leakage 48 for 503
Useless leakage 48 for 504
Useless leakage 48 for 505
Useless leakage 48 for 506
Useless leakage 48 for 507
Useless leakage 48 for 508
Useless leakage 48 for 509
Useless leakage 48 for 510
Useless leakage 48 for 511
Useless leakage 48 for 512
Useless leakage 48 for 513
Useless leakage 48 for 514
Useless leakage 20 for 515
Useless leakage 48 for 516
Useless leakage 48 for 517
Useless leakage 48 for 518
Useless leakage 48 for 519
Useful leak at 520 for key byte 15 = c5-> already known
Current rk10 = 13 11 1d 7f e3 94 00 17 f3 07 a7 8b 4d 2b 30 c5
Useful leak at 521 for key byte 6 = 4a-> NEW!
All round key bytes found after 522 plaintexts
Current rk10 = 13 11 1d 7f e3 94 4a 17 f3 07 a7 8b 4d 2b 30 c5
   sgx-dsn:~/0xbadc0de-poc/intel-sgx-sdk-strlen-ssa$
```

00:06 00:06

References i

A. C. Aldaya and B. B. Brumley.
When one vulnerable primitive turns viral: Novel single-trace attacks on ECDSA and RSA.
IACR Transactions on Cryptographic Hardware and Embedded Systems, pp. 196–221, 2020.

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