Reflections on Trusting Trusted Execution

The Story of Microarchitectural Attacks and Defenses

Jo Van Bulck

COSIC Course on Cryptography and Cyber Security, Leuven, July 4, 2024

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DistriNet
KU LEUVEN

Fast and Efficient Implementation of Homomorphic Encryption?

9:00-9:30	Hardware security: state of the art	Ingrid Verbauwhede, COSIC
9:30-10:30	Homomorphic Encryption (focus point to be added)	Jan-Pieter D'Anvers, COSIC
10:30-11:00	Coffee break (Landbouwinstituut Hoofdgebouw)	
11:00-11:45	Post-quantum cryptography: NIST standardization, Present and Future	Angshuman Karmakar, IIT Kanpur
11:45-12:30	Microarchitectural attacks	Jo Van Bulck, DistriNet
12:30-14:00	Lunch	
14:00-15:00	Side Channel + Lattice Based Systems	Elisabeth Oswald + Matthias Steiner, University of Klagenfurt
15:00-16:00	Homomorphic Encryption: the practical side	Johannes Mono, Ruhr University Bochum
16:00-16:30	Coffee break (Landbouwinstituut Hoofdgebouw)	
16:30-17:30	Fast GPU implementation of the BFV and CKKS homomorphic encryption schemes	Erkay Savas, Sabanci University

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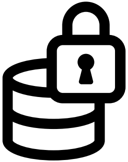
How does today's topic fit in?

The Big Picture: Protecting Private Data

Data in transit

Data in use



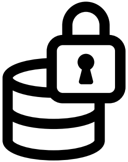
Data at rest

The Big Picture: Protecting Private Data

Data in transit

- ✓ SSL/TLS etc.

Data in use



Data at rest

- ✓ Full disk encryption

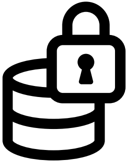
The Big Picture: Protecting Private Data

Data in transit

- SSL/TLS etc.

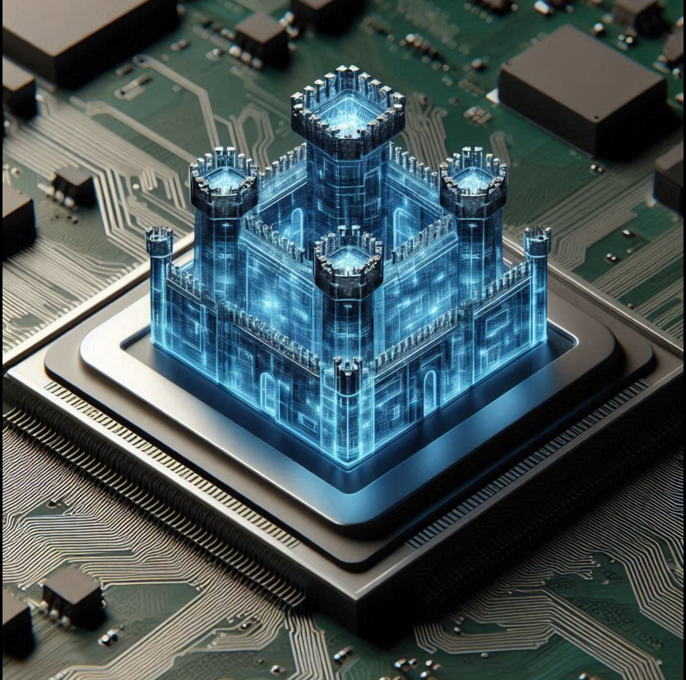
Data in use

- **Homomorphic encryption?**
- **Trusted Execution?**
  - = *Confidential Computing*
  - = *Hardware Enclaves*

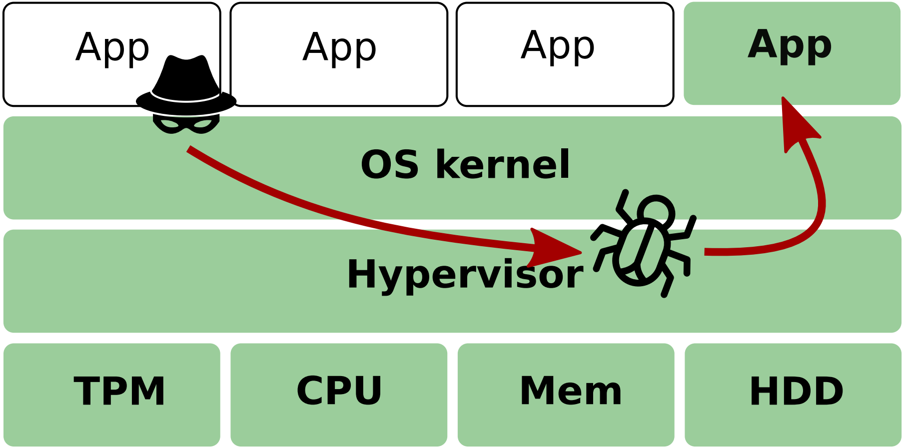


Data at rest

- Full disk encryption

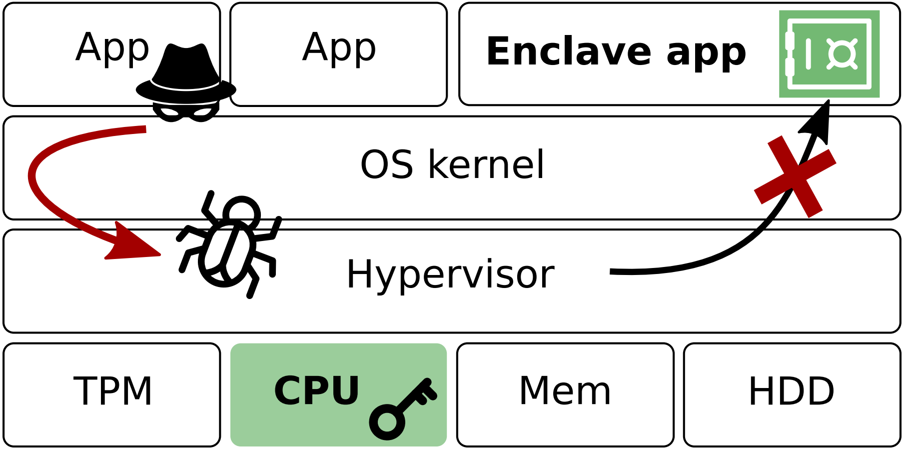

DALL·E 3

The Big Picture: Reducing Attack Surface with Enclaves



Traditional **layered designs:** Large trusted computing base

The Big Picture: Reducing Attack Surface with Enclaves



Intel SGX promise: Hardware-level **isolation and attestation**

The Rise of Trusted Execution Environments

- 2004: ARM TrustZone
- 2015: Intel Software Guard Extensions (SGX)
- 2016: AMD Secure Encrypted Virtualization (SEV)
- 2018: IBM Protected Execution Facility (PEF)
- 2020: AMD SEV with Secure Nested Paging (SEV-SNP)
- 2022: Intel Trust Domain Extensions (TDX)
- 2024: ARM Confidential Computing Architecture (CCA)

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TEEs are here to stay...

Hardware Enclaves vs. Homomorphic Encryption?

Confidential Computing is available in production today. It provides practical, useful protections for data in use and in a few years, we should see Homomorphic Encryption become available for production

🌐 https://confidentialcomputing.io/2023/03/29/confidential-computing-and-homomorphic-encryption/

Hardware Enclaves vs. Homomorphic Encryption?

	Homomorphic Encryption	Confidential Computing
Data Integrity	X	√
Data Confidentiality	√	√
Code Integrity	X	√
Code Confidentiality	X	√
Authenticated Launch	X	varies
Attestability	X	√
Recoverability	X	√

Confidential Computing is already in active use, while Homomorphic Encryption is still in the experimentation phase

https://www.edgeless.systems/blog/the-differences-between-homomorphic-encryption-he-the-differences-between-homomorphic

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Data Integrity	X	√
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Code Integrit	[illegible]	[illegible]
Code Confide	[illegible]	[illegible]
Authenticated Launch	X	varies
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Recoverability	X	√

Mathematical guarantees!

Real-world implementation?

Confidential Computing is already in active use, while Homomorphic Encryption is still in the experimentation phase

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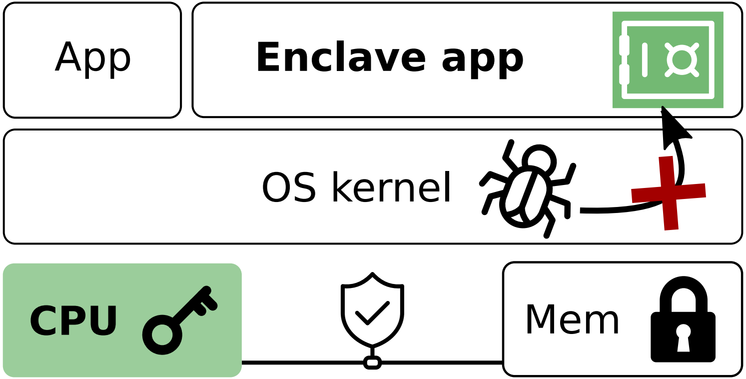
Overview: Architectural Enclave Isolation

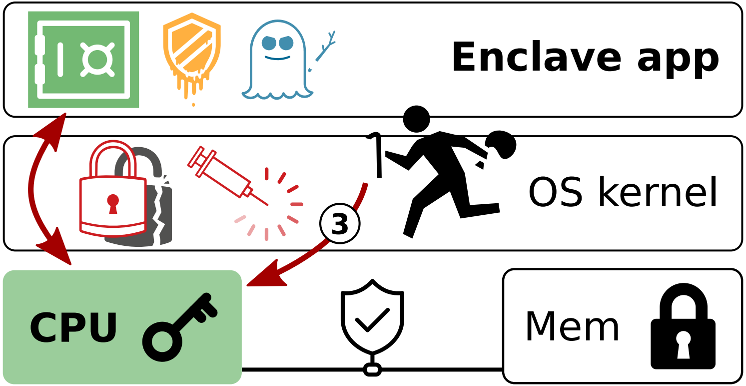


Architectural promise: Transparent data-in-use protection against privileged software adversaries

Overview: Microarchitectural Side-Channel Attacks (today)

Microarchitectural reality: Novel side channels to spy on enclave-CPU interaction metadata

Overview: Transient-Execution Attacks (not today)



Microarchitectural reality: Direct data extraction via transient-execution attacks...

DALL·E 3

A Note on SGX Side-Channel Attacks (Intel)

Protection from Side-Channel Attacks

Intel® SGX does not provide explicit protection from side-channel attacks. It is the enclave developer's responsibility to address side-channel attack concerns.

In general, enclave operations that require an OCall, such as thread synchronization, I/O, etc., are exposed to the untrusted domain. If using an OCall would allow an attacker to gain insight into enclave secrets, then there would be a security concern. This scenario would be classified as a side-channel attack, and it would be up to the ISV to design the enclave in a way that prevents the leaking of side-channel information.

An attacker with access to the platform can see what pages are being executed or accessed. This side-channel vulnerability can be mitigated by aligning specific code and data blocks to exist entirely within a single page.

More important, the application enclave should use an appropriate crypto implementation that is side channel attack resistant inside the enclave if side-channel attacks are a concern.

software.intel.com/en-us/node/703016

Vulnerable Patterns: Secret-Dependent Code/Data Accesses

```c
void secret_vote(char candidate)
{
    if (candidate == 'a')
        vote_candidate_a();
    else
        vote_candidate_b();
}
```

```c
int secret_lookup(int s)
{
    if (s > 0 && s < ARRAY_LEN)
        return array[s];
    return -1;

}
```

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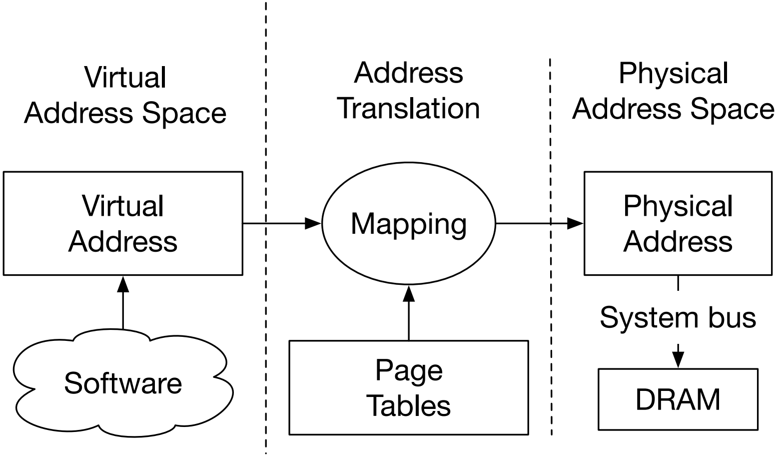
```

What are new ways for privileged adversaries to create an "oracle" for enclave code+data memory accesses?

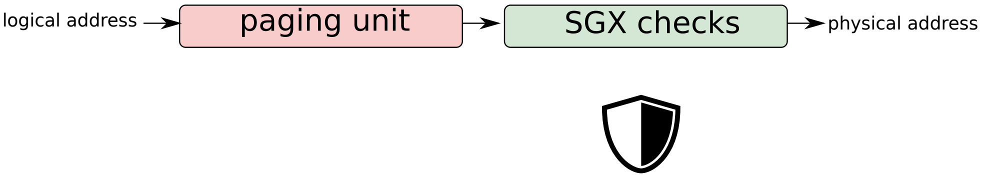
Idea #1: Monitoring Address Translation

The Virtual Memory Abstraction



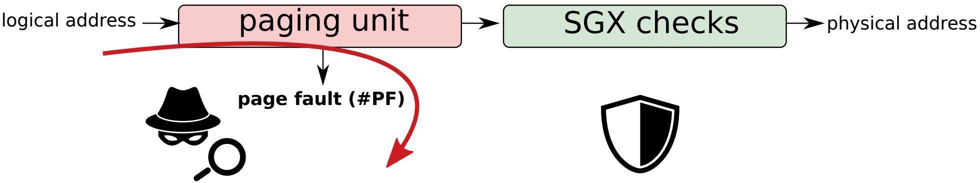
Costan et al. "Intel SGX explained", IACR 2016.

Intel SGX: Page Faults as a Side Channel



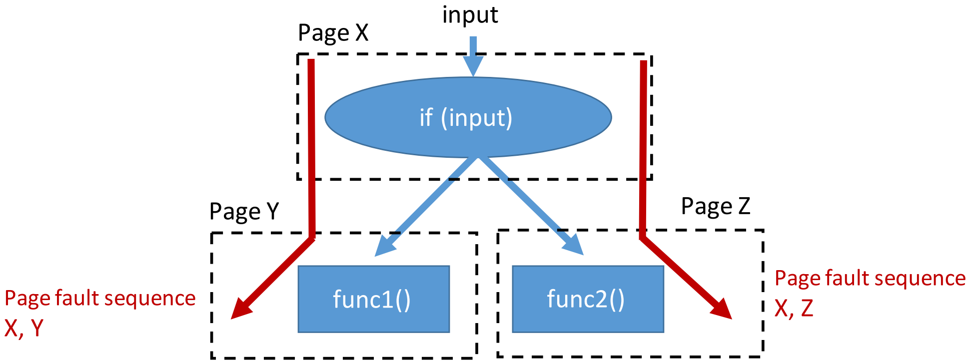
SGX machinery protects against direct address remapping attacks

Intel SGX: Page Faults as a Side Channel



...but untrusted address translation may **fault(!)**

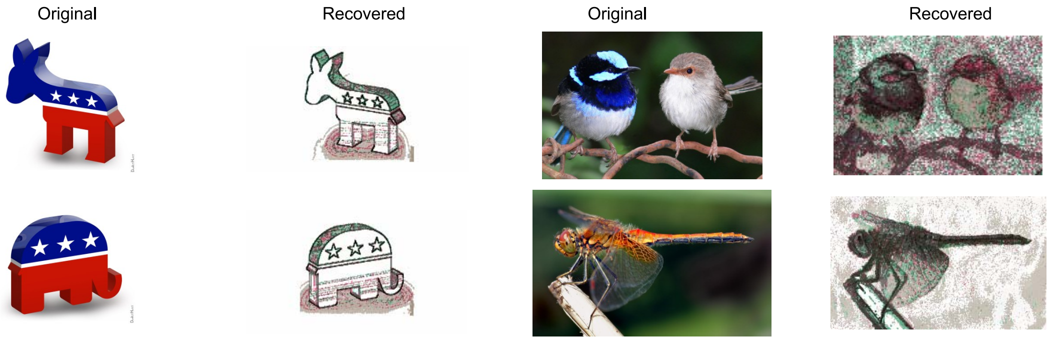
Intel SGX: Page Faults as a Side Channel



🗋 Xu et al.: "Controlled-channel attacks: Deterministic side channels for untrusted operating systems", Oakland 2015.

⟹ Page fault traces leak **private control data/flow**

Page Table-Based Attacks in Practice



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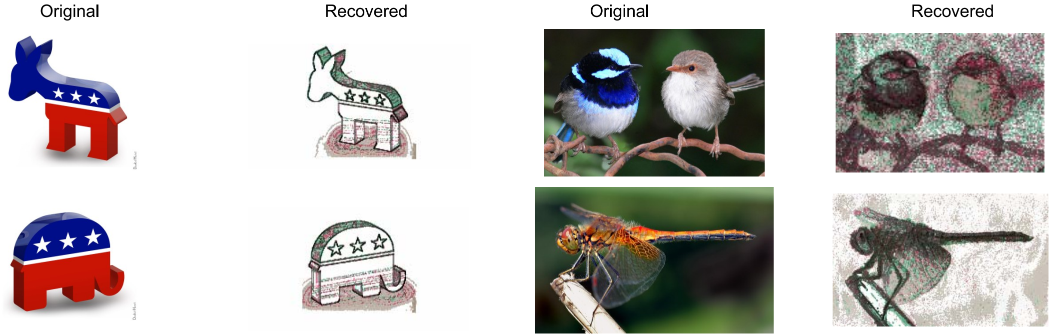
⇒ **Low-noise, single-run** exploitation of legacy applications

Page Table-Based Attacks in Practice



🗋 Xu et al.: "Controlled-channel attacks: Deterministic side channels for untrusted operating systems", Oakland 2015.

. . . but a coarse-grained **4 KiB spatial granularity**

Idea #2: Improving Temporal Resolution

Intel's Note on Side-Channel Attacks (Revisited)

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software.intel.com/en-us/node/703016

Temporal Resolution Limitations for the Page-Fault Oracle

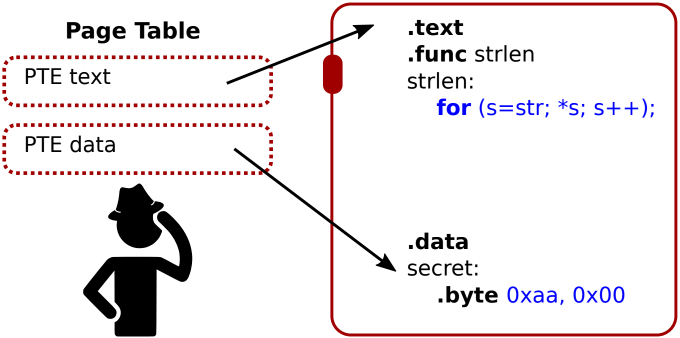
```c
size_t strlen (char *str)
{
  char *s;

  for (s = str; *s; ++s);
  return (s - str);
}
```

```
    mov   %rdi,%rax
1:  cmpb  $0x0,(%rax)
    je    2f
    inc   %rax
    jmp   1b
2:  sub   %rdi,%rax
    retq
```

⇒ tight loop: 4 instructions, single memory operand, single code + data page

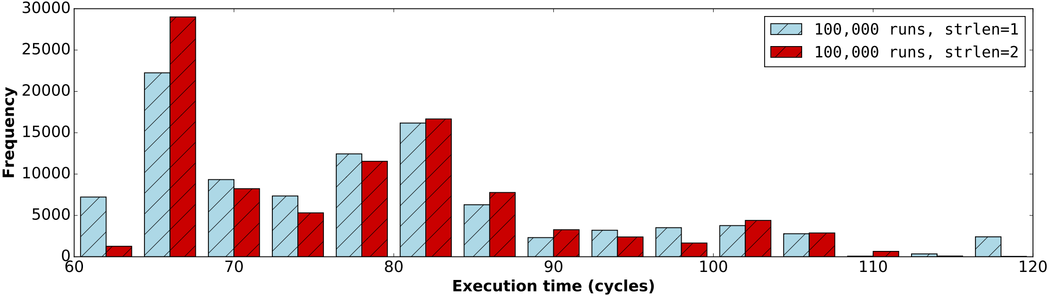
Temporal Resolution Limitations for the Page-Fault Oracle



Counting `strlen` loop iterations?

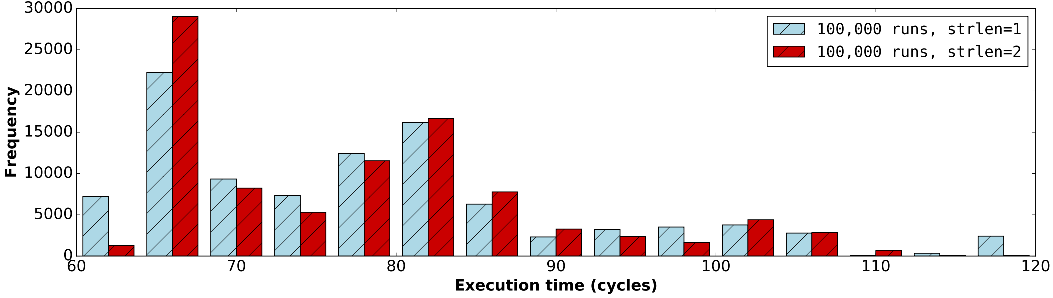
Progress requires both pages present (non-faulting) ↔ page fault oracle

Building the `strlen()` side-channel oracle with execution timing?



Building the `strlen()` side-channel oracle with execution timing?

Too noisy: Modern x86 processors are lightning fast. . .



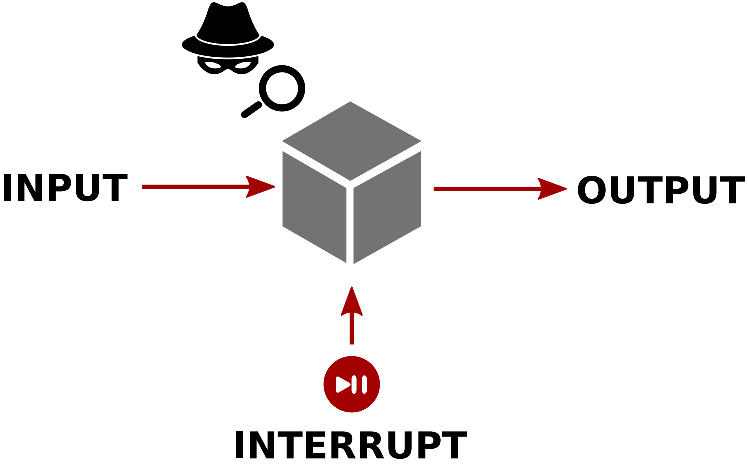
Challenge: Side-channel Sampling Rate

Slow
shutter speed

Medium
shutter speed

Fast
shutter speed

SGX-Step: Executing Enclaves one Instruction at a Time



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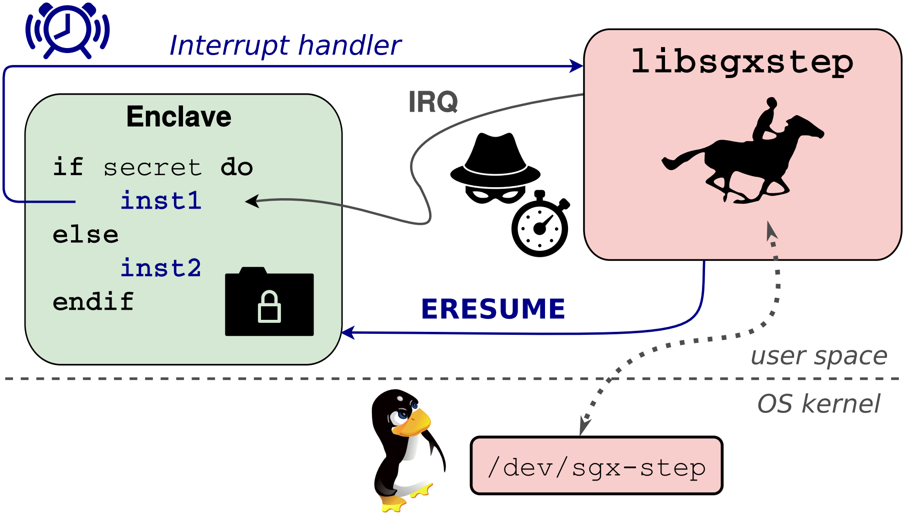


Van Bulck et al., "SGX-Step: A Practical Attack Framework for Precise Enclave Execution Control", SysTEX 2017.

SGX-Step demo: Building a `memcmp()` Password Oracle

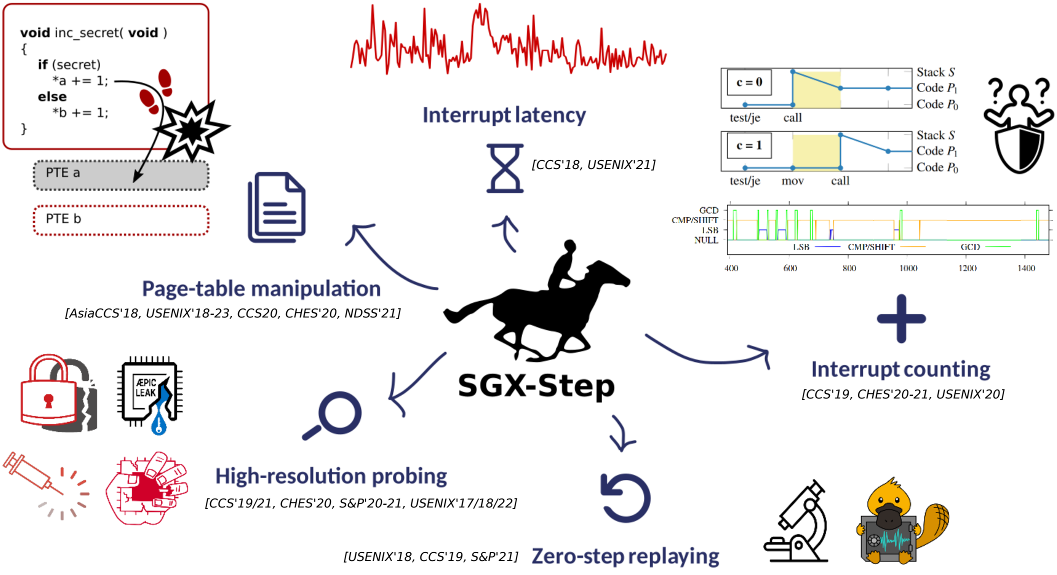
```
[idt.c] DTR.base=0xfffffe0000000000/size=4095 (256 entries)
[idt.c] established user space IDT mapping at 0x7f7ff8e9a000
[idt.c] installed asm IRQ handler at 10:0x56312d19b000
[idt.c] IDT[ 45] @0x7f7ff8e9a2d0 = 0x56312d19b000 (seg sel 0x10); p=1; dpl=3; type=14; ist=0
[file.c] reading buffer from '/dev/cpu/1/msr' (size=8)
[apic.c] established local memory mapping for APIC_BASE=0xfee00000 at 0x7f7ff8e99000
[apic.c] APIC_ID=2000000; LVTT=400ec; TDCR=0
[apic.c] APIC timer one-shot mode with division 2 (lvtt=2d/tdcr=0)

--------------------------------------------------------------------------------
[main.c] recovering password length
--------------------------------------------------------------------------------

[attacker] steps=15; guess='******'
[attacker] found pwd len = 6

--------------------------------------------------------------------------------
[main.c] recovering password bytes
--------------------------------------------------------------------------------

[attacker] steps=35; guess='SECRET' --> SUCCESS

[apic.c] Restored APIC_LVTT=400ec/TDCR=0)
[file.c] writing buffer to '/dev/cpu/1/msr' (size=8)
[main.c] all done; counted 2260/2183 IRQs (AEP/IDT)
jo@breuer:~/sgx-step-demo$
```

SGX-Step: Enabling a New Line of High-Resolution Attacks

Yr	Venue	Paper	Step	Use Case	Drv
'15	S&P	Ctrl channel [XCP15]	~ Page	*Probe* (page fault)	✓
'16	ESORICS	AsyncShock [WKPK16]	~ Page	*Exploit* (mem safety)	–
'17	CHES	CacheZoom [MIE17]	✗ >1	*Probe* (L1 cache)	✓
'17	ATC	Hahnel et al. [HCP17]	✗ 0 - >1	*Probe* (L1 cache)	✓
'17	USENIX	BranchShadow [LSG+17]	✗ 5 - 50	*Probe* (BPU)	✗
'17	USENIX	Stealthy PTE [VBWK+17]	~ Page	*Probe* (page table)	✓
'17	USENIX	DarkROP [LJJ+17]	~ Page	*Exploit* (mem safety)	✓
'17	SysTEX	SGX-Step [VBPS17]	✓ 0 - 1	*Framework*	✓
'18	ESSoS	Off-limits [GVBPS18]	✓ 0 - 1	*Probe* (segmentation)	✓
'18	AsiaCCS	Single-trace RSA [WSB18]	~ Page	*Probe* (page fault)	✓
'18	USENIX	Foreshadow [VBMW+18]	✓ 0 - 1	*Probe* (transient exec)	✓
'18	EuroS&P	SgxPectre [CCX+19]	~ Page	*Exploit* (transient)	✓
'18	CHES	CacheQuote [DDME+18]	✗ >1	*Probe* (L1 cache)	✓
'18	ICCD	SGXlinger [HZDL18]	✗ >1	*Probe* (IRQ latency)	✗
'18	CCS	Nemesis [VBPS18]	✓ 1	*Probe* (IRQ latency)	✓
'19	USENIX	Spoiler [IMB+19]	✓ 1	*Probe* (IRQ latency)	✓
'19	CCS	ZombieLoad [SLM+19]	✓ 0 - 1	*Probe* (transient exec)	✓
'19	CCS	Fallout [CGG+19]	–	*Probe* (transient exec)	✓
'19	CCS	Tale of 2 worlds [VBOM+19]	✓ 1	*Exploit* (mem safety)	✓
'19	ISCA	MicroScope [SYG+19]	~ 0 - Page	*Framework*	✗
'20	CHES	Bluethunder [HMW+20]	✓ 1	*Probe* (BPU)	✓
'20	USENIX	Big troubles [WSBS19]	~ Page	*Probe* (page fault)	✓
'20	S&P	Plundervolt [MOG+20]	–	*Exploit* (undervolt)	✓
'20	CHES	Viral primitive [AB20]	✓ 1	*Probe* (IRQ count)	✓
'20	USENIX	CopyCat [MVBH+20]	✓ 1	*Probe* (IRQ count)	✓
'20	S&P	LVI [VBMS+20]	✓ 1	*Exploit* (transient)	✓

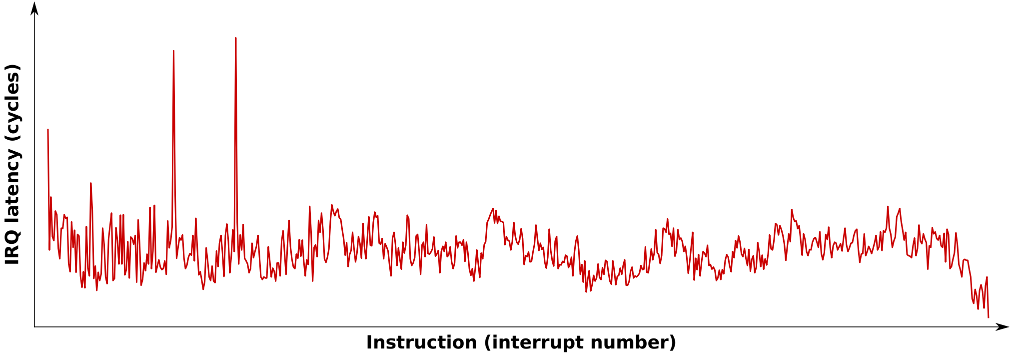
Yr	Venue	Paper	Step	Use Case	Drv
'20	CHES	A to Z [AGB20]	~ Page	*Probe* (page fault)	✓
'20	CCS	Déjà Vu NSS [uHGDL+20]	~ Page	*Probe* (page fault)	✓
'20	MICRO	PTHammer [ZCL+20]	–	*Probe* (page walk)	✓
'21	USENIX	Frontal [PSHC21]	✓ 1	*Probe* (IRQ latency)	✓
'21	S&P	CrossTalk [RMR+21]	✓ 1	*Probe* (transient exec)	✓
'21	CHES	Online template [AB21]	✓ 1	*Probe* (IRQ count)	✓
'21	NDSS	SpeechMiner [XZT20]	–	*Framework*	✓
'21	S&P	Platypus [LKO+21]	✓ 0 - 1	*Probe* (voltage)	✓
'21	DIMVA	Aion [HXCL21]	✓ 1	*Probe* (cache)	✓
'21	CCS	SmashEx [CYS+21]	✓ 1	*Exploit* (mem safety)	✓
'21	CCS	Util::Lookup [SBWE21]	✓ 1	*Probe* (L3 cache)	✓
'22	USENIX	Rapid prototyping [ESSG22]	✓ 1	*Framework*	✓
'22	CT-RSA	Kalyna expansion [CGYZ22]	✓ 1	*Probe* (L3 cache)	✓
'22	SEED	Enclyzer [ZXTZ22]	–	*Framework*	✓
'22	NordSec	Self-monitoring [LBA22]	~ Page	*Defense* (detect)	✓
'22	AutoSec	Robotic vehicles [LS22]	✓ 1 - >1	*Exploit* (timestamp)	✓
'22	ACSAC	MoLE [LWM+22]	✓ 1	*Defense* (randomize)	✓
'22	USENIX	AEPIC [BKS+22]	✓ 1	*Probe* (I/O device)	✓
'22	arXiv	Confidential code [PSL+22]	✓ 1	*Probe* (IRQ latency)	✓
'23	ComSec	FaultMorse [HZL+23]	~ Page	*Probe* (page fault)	✓
'23	CHES	HQC timing [HSC+23]	✓ 1	*Probe* (L3 cache)	✓
'23	ISCA	Belong to us [YJF23]	✓ 1	*Probe* (BPU)	✓
'23	USENIX	BunnyHop [ZTO+23]	✓ 1	*Probe* (BPU)	✓
'23	USENIX	DownFall [Mog23]	✓ 0 - 1	*Probe* (transient exec)	✓
'23	USENIX	AEX-Notify [CVBC+23]	✓ 1	*Defense* (prefetch)	✓

SGX-Step: A Versatile Open-Source Attack Toolkit



Nemesis: Extracting Interrupt Latency Traces with SGX-Step

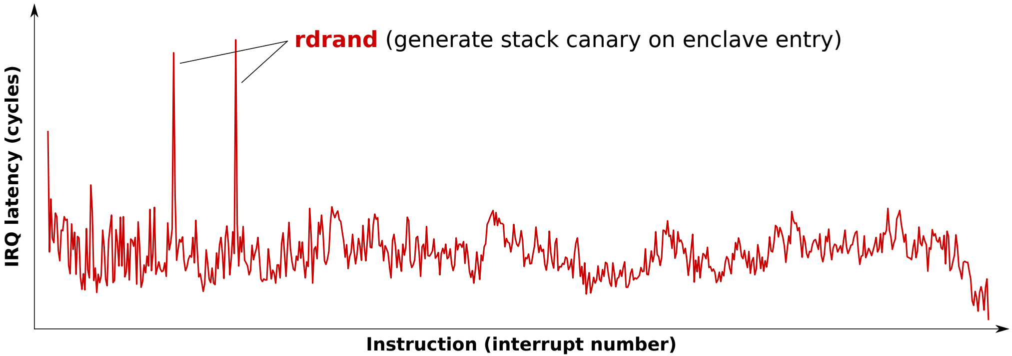
Enclave x-ray: IRQ latency leaks instruction-level μ-arch timing!



Van Bulck et al. "Nemesis: Studying Microarchitectural Timing Leaks in Rudimentary CPU Interrupt Logic", CCS 2018..

Nemesis: Extracting Interrupt Latency Traces with SGX-Step

Enclave x-ray: Spotting high-latency instructions



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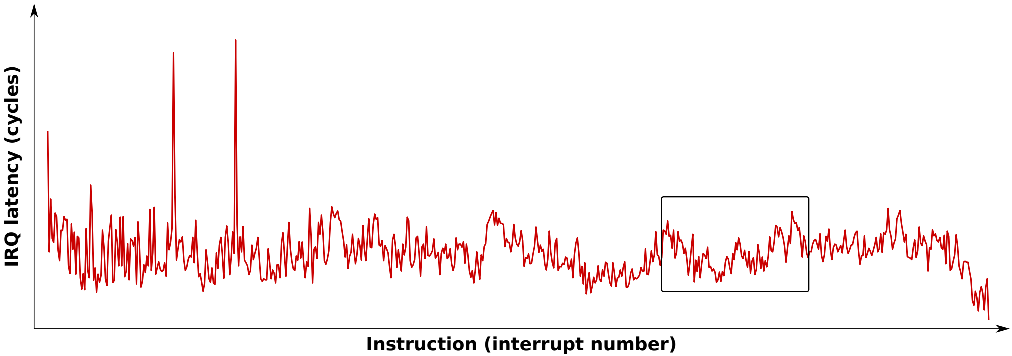
Nemesis: Extracting Interrupt Latency Traces with SGX-Step

Enclave x-ray: Zooming in on `bsearch` function



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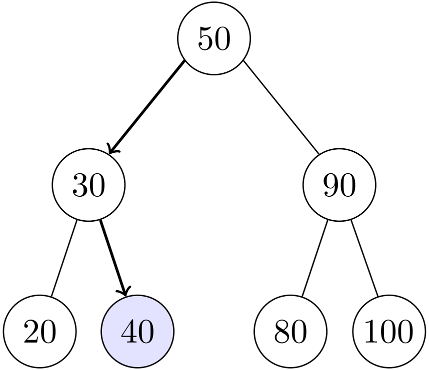
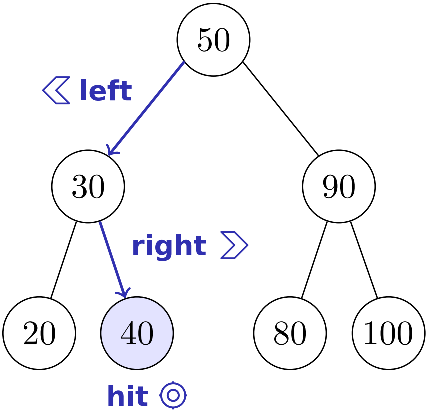
De-Anonymizing Enclave Lookups with Interrupt Latency

Binary search: Find 40 in $\{20, 30, 40, 50, 80, 90, 100\}$



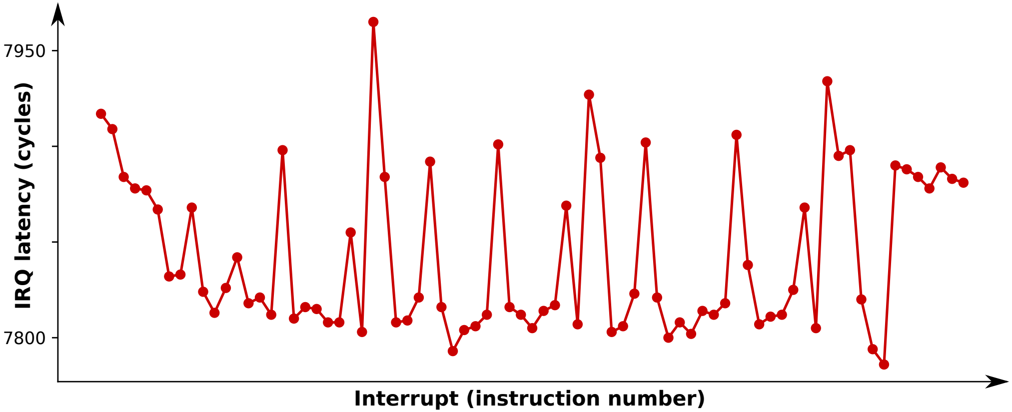
De-Anonymizing Enclave Lookups with Interrupt Latency

Adversary: Infer secret lookup in known array



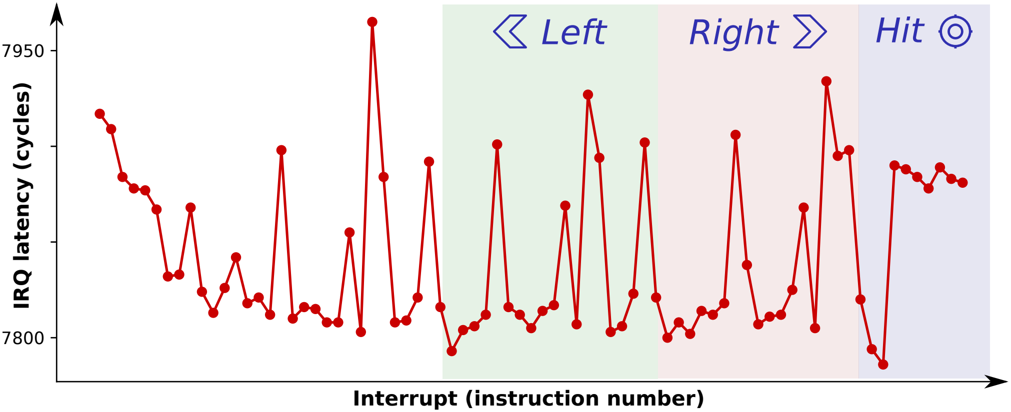
De-Anonymizing Enclave Lookups with Interrupt Latency

Goal: Infer lookup → reconstruct `bsearch` control flow



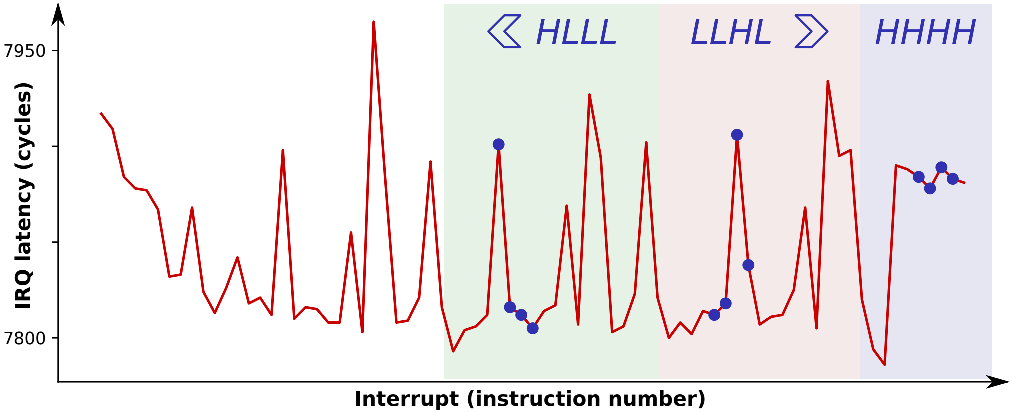
De-Anonymizing Enclave Lookups with Interrupt Latency

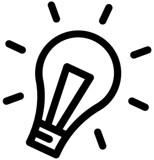
Goal: Infer lookup → reconstruct `bsearch` control flow



De-Anonymizing Enclave Lookups with Interrupt Latency

⇒ Sample **instruction latencies** in secret-dependent path





Idea #3: Interrupt Hardening

Hardening Enclaves against Interrupt-Driven Attacks

SGX-Step sets the **bar for adequate side-channel defenses!**

SGX-Step inspired several dedicated **hardware-software mitigations**

→ Several research prototypes on in-house secure Sancus processor

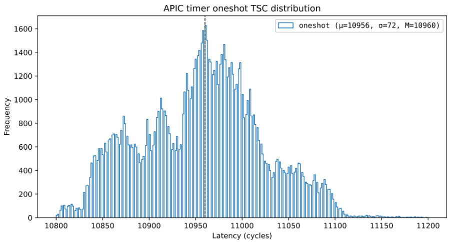
→ Collaboration with Intel on AEX-Notify: Included in recent processors

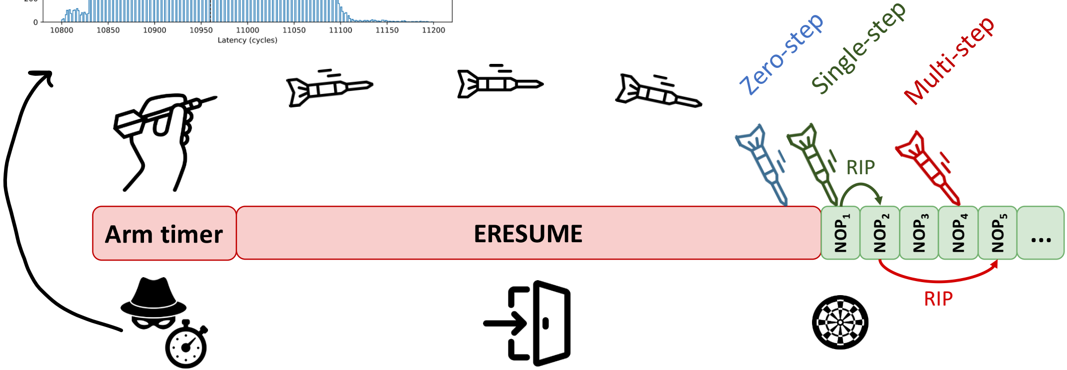
Busi et al., "Provably Secure Isolation for Interruptible Enclaved Execution on Small Microprocessors", CSF 2020..

Bognar et al., "MicroProfiler: Principled Side-Channel Mitigation through Microarchitectural Profiling", EuroS&P 2023..

Constable et al., "AEX-Notify: Thwarting Precise Single-Stepping Attacks through Interrupt Awareness for Intel SGX Enclaves", USENIX 2023..

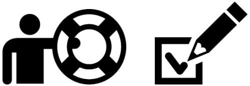
Root-causing SGX-Step: Aiming the timer interrupt

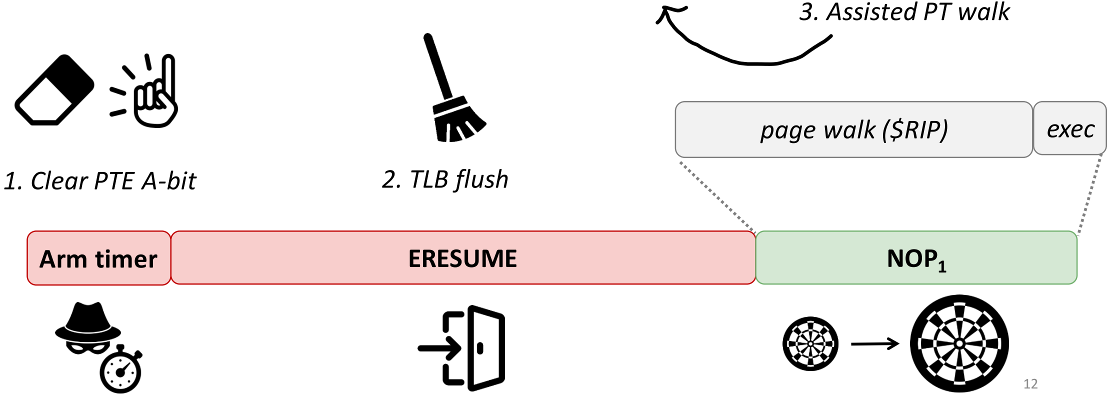




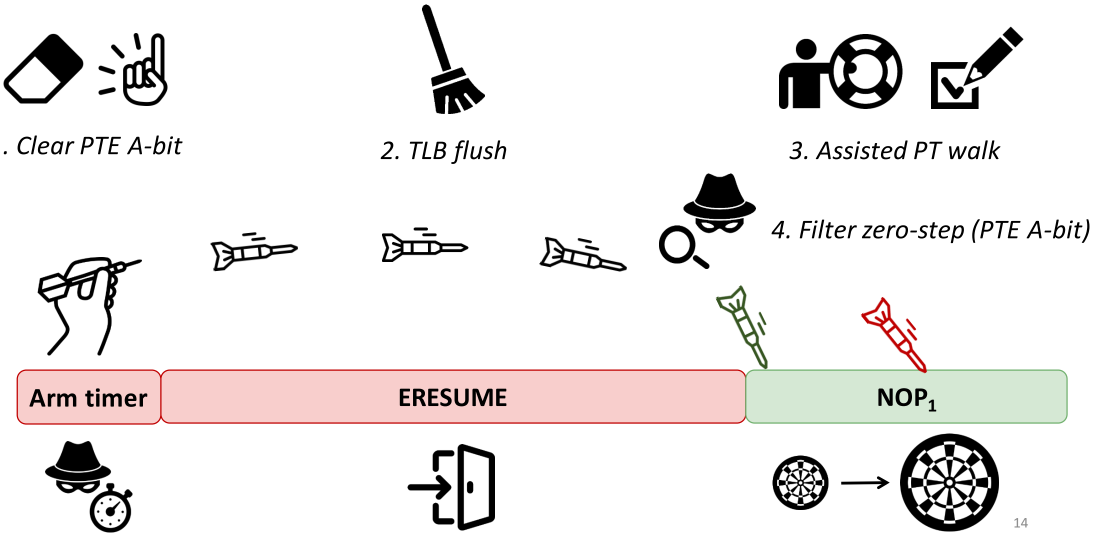
Root-causing SGX-Step: Microcode assists to the rescue!

PTE A-bit	Mean (cycles)	Stddev (cycles)
A=1	27	30
A=0	666	55

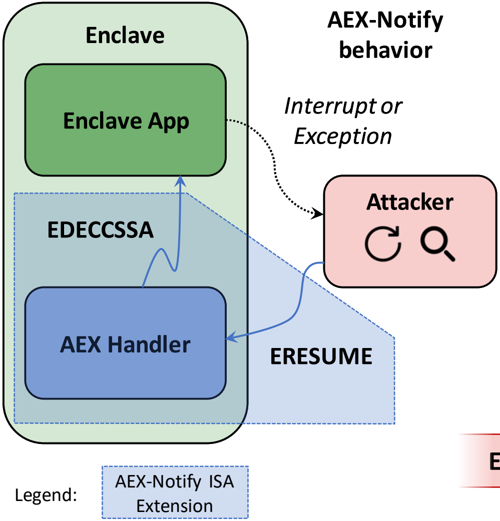


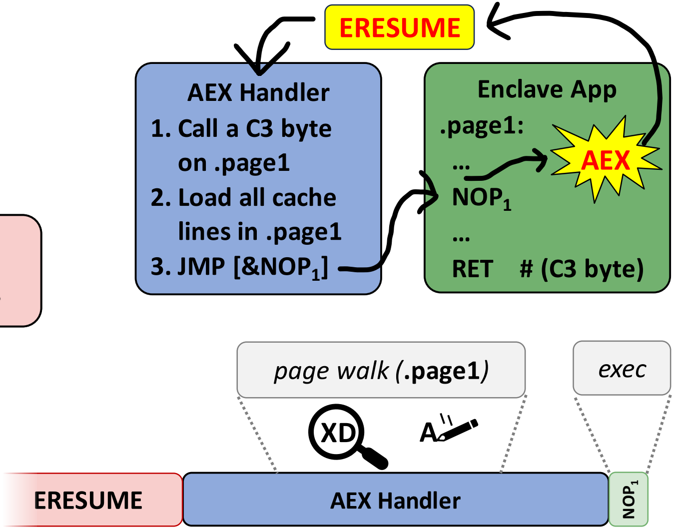


Root-causing SGX-Step: Microcode assists to the rescue!



AEX-Notify solution overview





intel.

CHAPTER 8
ASYNCHRONOUS ENCLAVE EXIT NOTIFY AND THE EDECCSSA USER LEAF FUNCTION

8.1 INTRODUCTION

Asynchronous Enclave Exit Notify (AEX-Notify) is an extension to Intel® SGX that allows Intel SGX enclaves to be notified after an asynchronous enclave exit (AEX) has occurred. EDECCSSA is a new Intel SGX user leaf function (ENCLU[EDECCSSA]) that can facilitate AEX notification handling, as well as software exception handling. This chapter provides information about changes to the Intel SGX architecture that support AEX-Notify and ENCLU[EDECCSSA].

The following list summarizes the a... details are provided in Section 8.3)...

- SECS.ATTRIBUTES.AEXNOTIFY...
- TCS.FLAGS.AEXNOTIFY: This e...
- SSA.GPRSGX.AEXNOTIFY: Enclave-writable byte that allows enclave software to dynamically enable/disable AEX notifications.

An AEX notification is delivered by ENCLU[ERESUME] when the following conditions are met:

SGX-Step led to **new x86 processor instructions!**

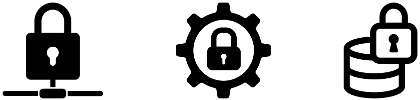
→ shipped in millions of devices ≥ 4th Gen Xeon CPU

Conclusions and Takeaway

⇒ **Trusted execution** environments (Intel SGX) $\neq$ perfect!

⇒ Subtle **side channels** can go a long way…

⇒ Scientific understanding driven by **attacker-defender race**



Conclusions and Takeaway

⟹ **Trusted execution** environments (Intel SGX) ≠ perfect!

⟹ Subtle **side channels** can go a long way...

⟹ Scientific understanding driven by **attacker-defender race**

Thank you! Questions?

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