Telling Your Secrets Without Page Faults:

Stealthy Page Table-Based Attacks on Enclaved Execution

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Frank Piessens[1] Raoul Strackx[1]

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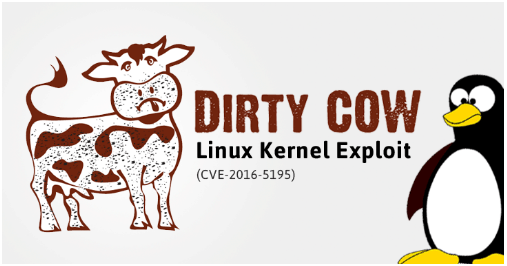
September 28, 2017

Road Map

thehackernews.com/2015/10/windows-patch-update.html

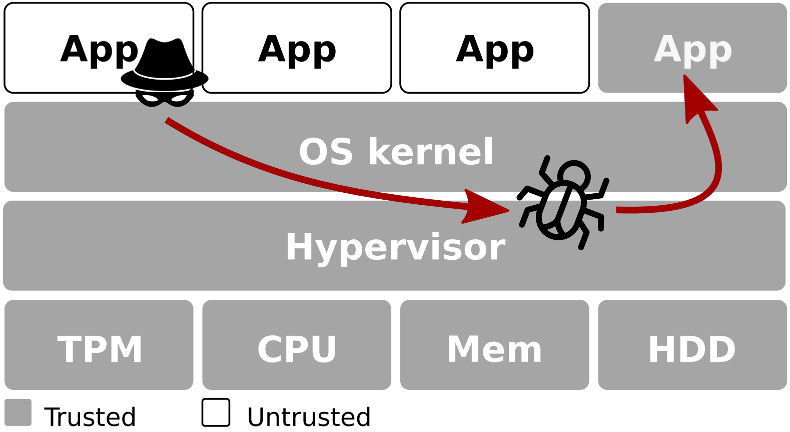
thehackernews.com/2017/06/cia-linux-hacking-tool-malware.html



thehackernews.com/2016/10/linux-kernel-exploit.html

thehackernews.com/2015/04/rootpipe-mac-os-x-vulnerability.html

Motivation: Application Attack Surface



Layered architecture → large **trusted computing base**

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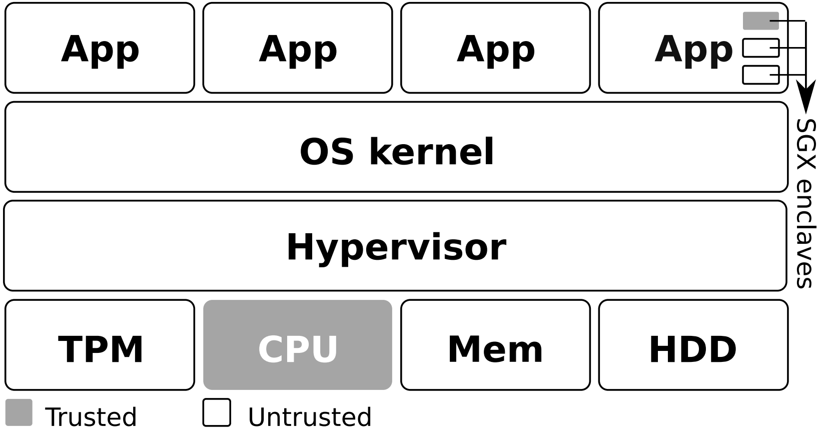

Intel SGX promise: hardware-level **isolation and attestation**

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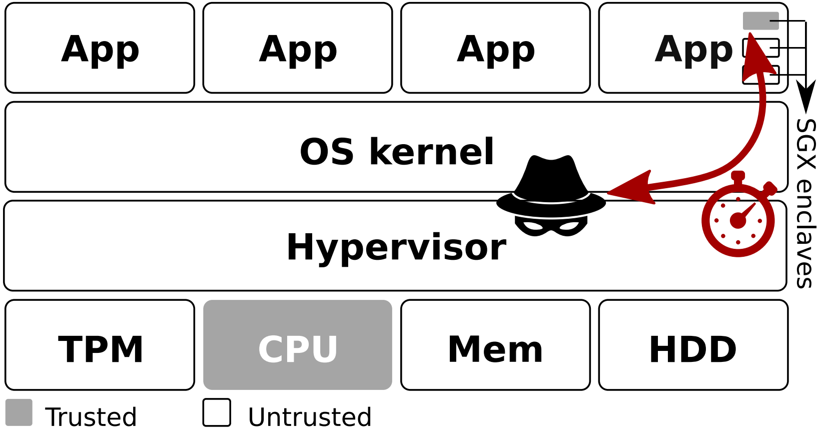
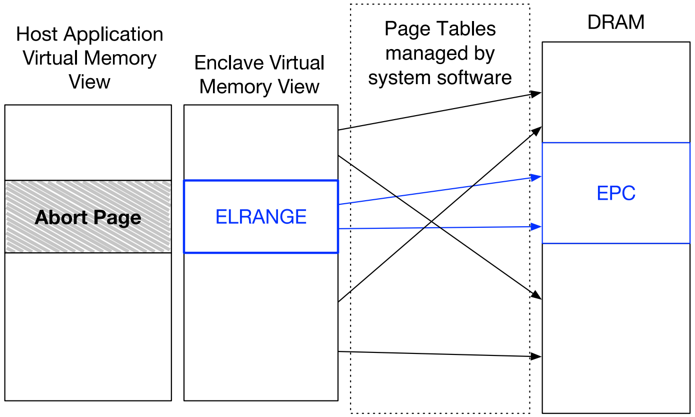


Untrusted OS → new class of powerful **side-channels**

Road Map

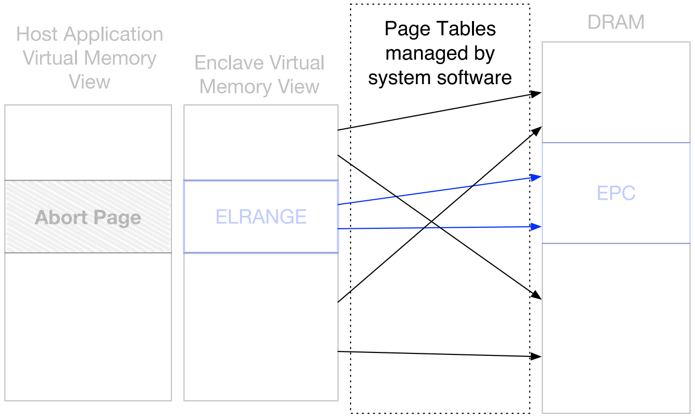
How Enclave Accesses are Enforced


Host Application Virtual Memory View
Abort Page
Enclave Virtual Memory View
ELRANGE
Page Tables managed by system software
DRAM
EPC

Costan et al. "Intel SGX explained", IACR 2016 [CD16]

How Enclave Accesses are Enforced

Note: Untrusted OS controls *virtual-to-physical mapping*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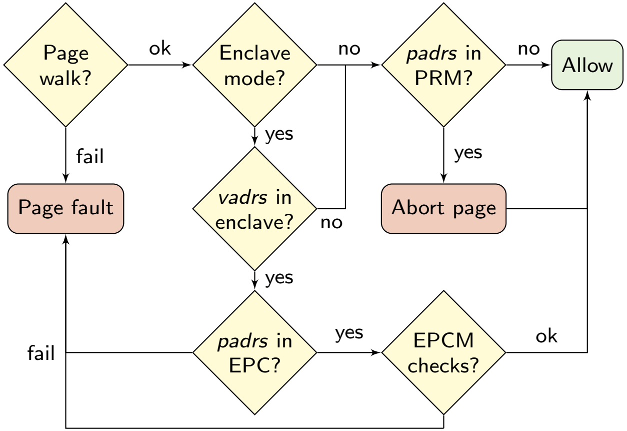
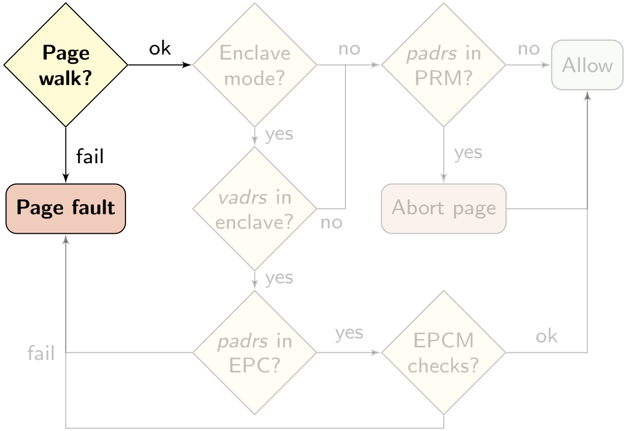
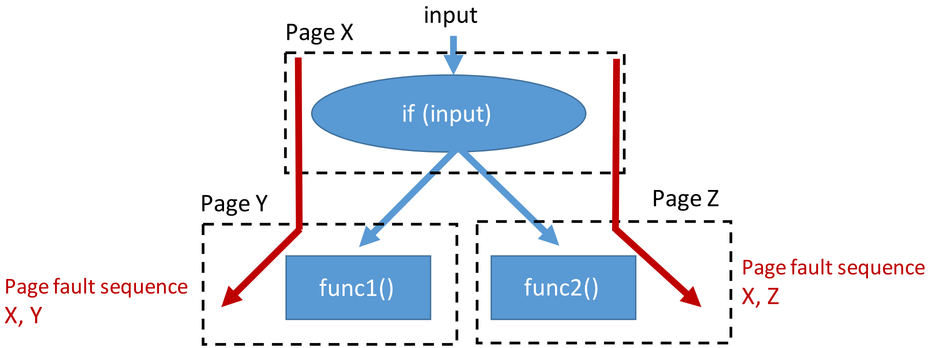


How Enclave Accesses are Enforced

Note: Additional checks *after* address translation



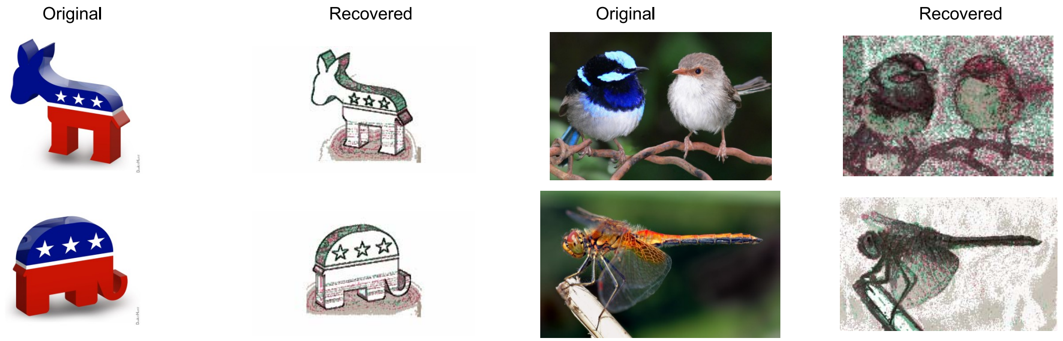
Page Faults as a Side-Channel



Xu et al.: "Controlled-channel attacks: Deterministic side channels for untrusted operating systems", Oakland 2015 [XCP15]

⇒ *Page fault traces leak private control flow/data accesses*

Page Faults as a Side-Channel



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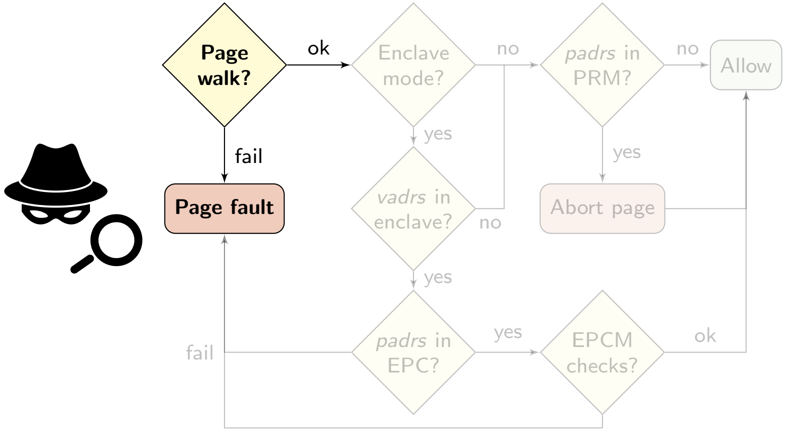
⇒ *Low-noise, single-run exploitation of legacy applications*

Current Solutions: Hiding Enclave Page Faults



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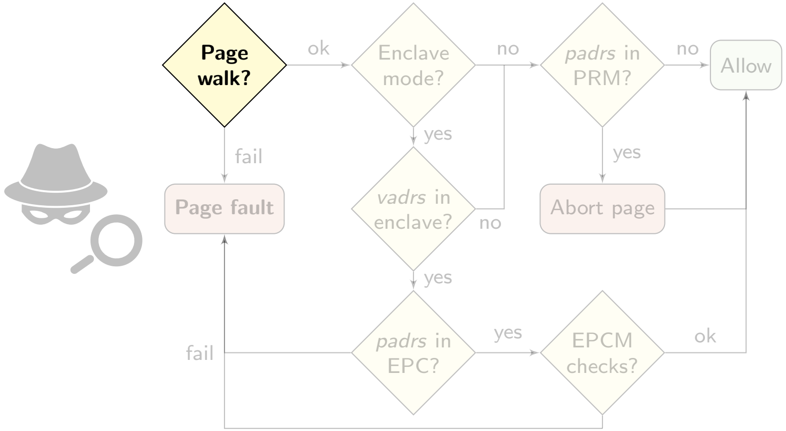

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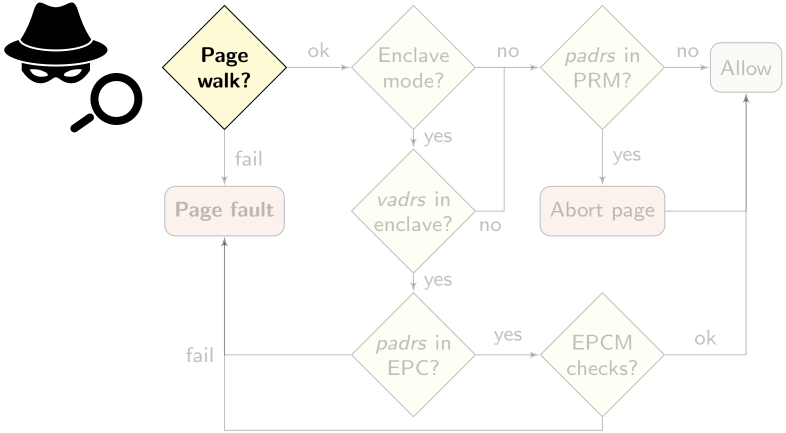

Defenses do not hold when attacker learns page accesses without triggering faults!

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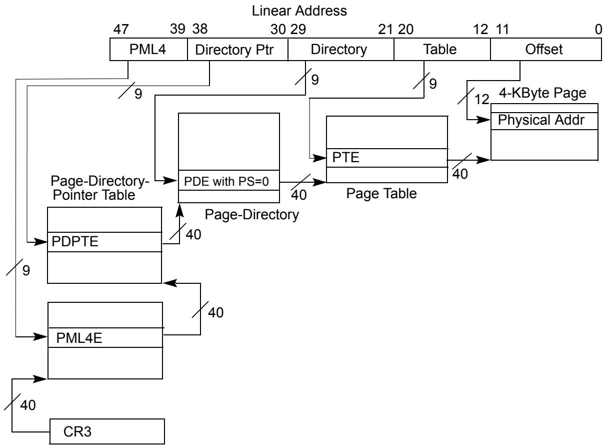

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Road Map

SGX Side-Channel Leakage: Page Table Entries

1. Attack vector: PTE **status flags**:
   - A(ccessed) bit
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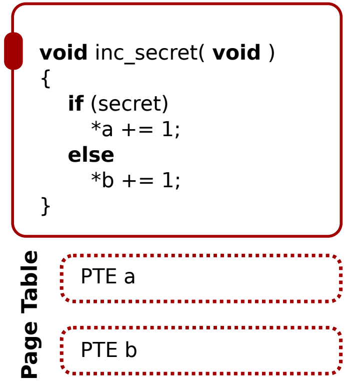

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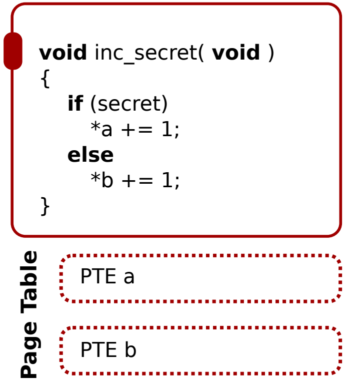

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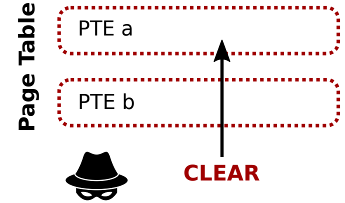

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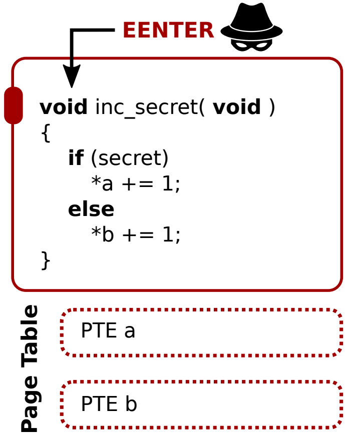

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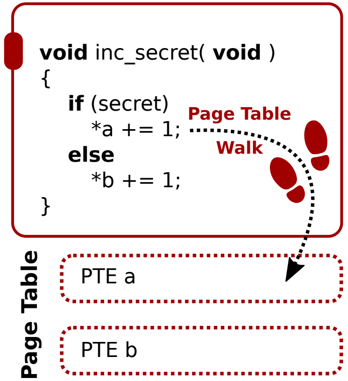
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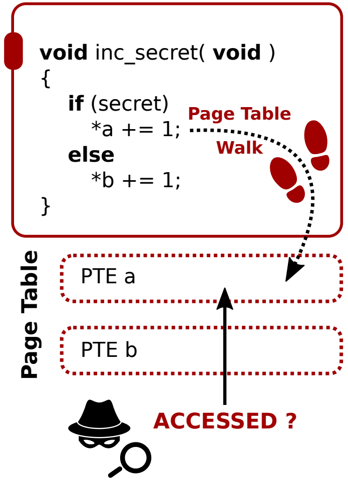

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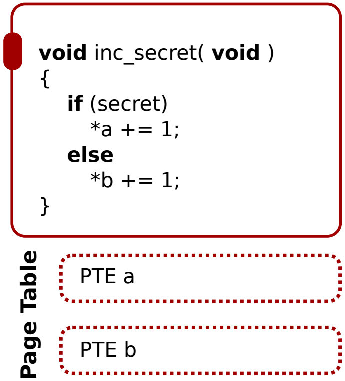

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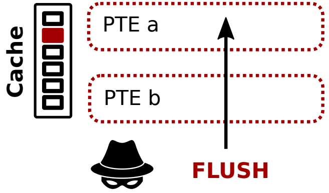

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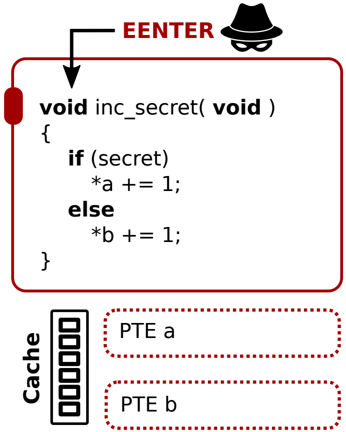

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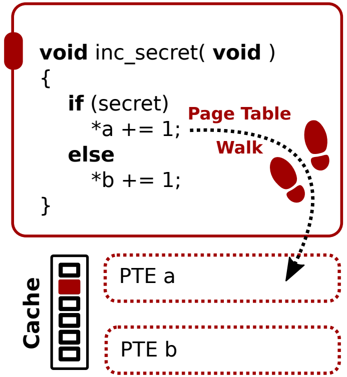

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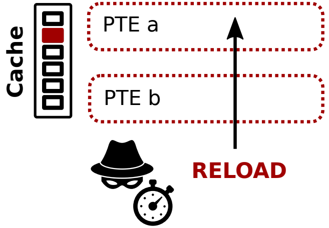

#PF-Less Challenges: Monitoring Repeated Accesses

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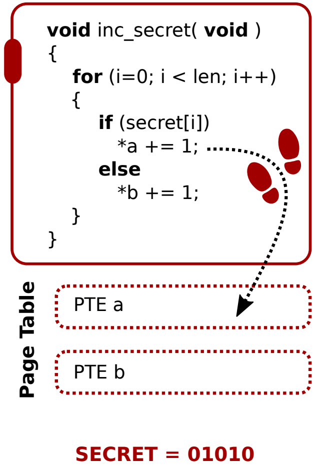

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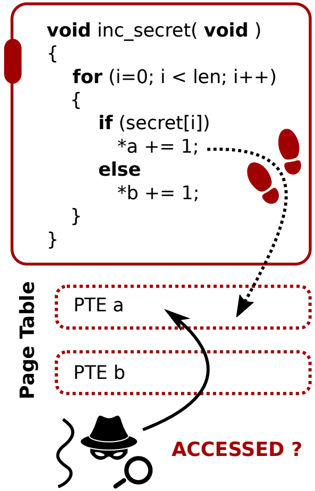

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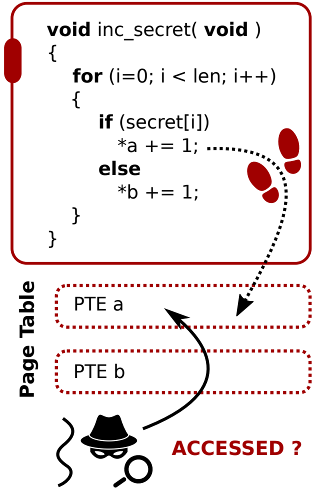

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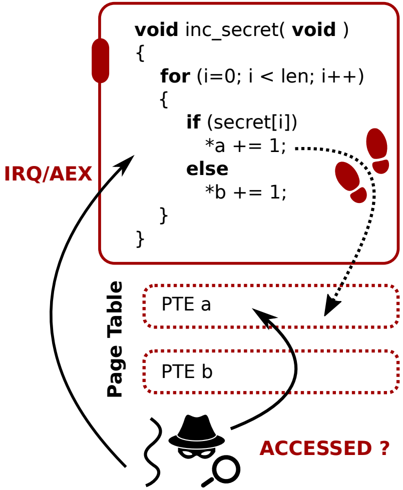
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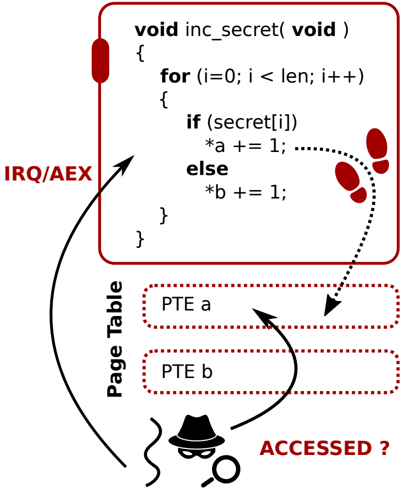

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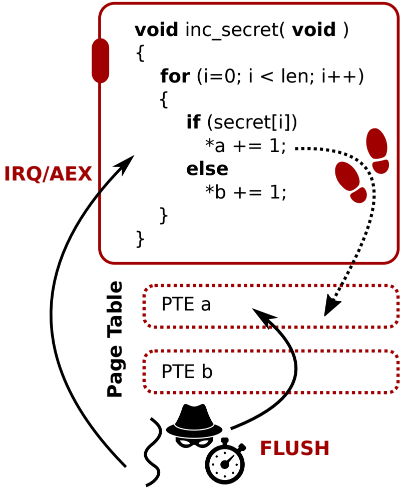
   ⇝ Precise **Flush+Flush** technique



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PTE Flush+Flush: A High-Resolution, Low-Latency Channel

Resolution Challenge

$\exists$ access **detection latency** $\leftrightarrow$ #PF-attacks

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Interrupt granularity:

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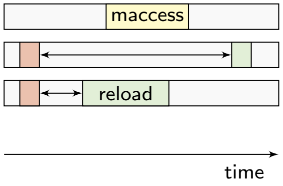
- ☹ Flush+Reload: might miss victim access (TLB!)

(a) Victim PTE access

(b) Flush+Reload hit

(c) Flush+Reload miss



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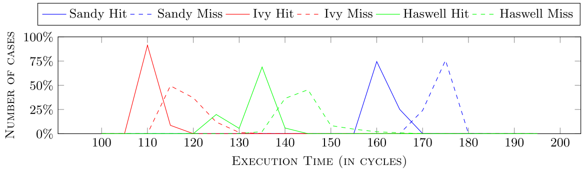

Gruss et al. "Flush+Flush: a fast and stealthy cache attack", DIMVA 2016 [GMWM16]

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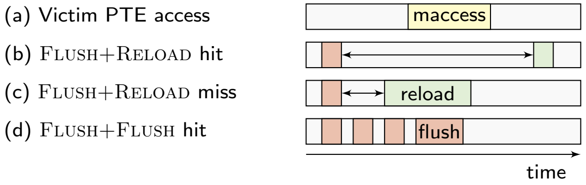
- ☺ Flush+Flush: interrupt *within trigger instruction* ($> 99.8\%$)



Attacking Libgcrypt EdDSA

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if (mpi_is_secure (scalar)) {
    /* If SCALAR is in secure memory we assume that it is the
       secret key we use constant time operation. */
    point_init (&tmppnt);

    for (j=nbits-1; j >= 0; j--) {
        _gcry_mpi_ec_dup_point (result, result, ctx);
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        point_swap_cond (result, &tmppnt, mpi_test_bit (scalar, j), ctx);
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EdDSA secret scalar *not* stored in "secure memory" !

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Secret-dependent control flow

Attacking Libgcrypt EdDSA: A/D Channel

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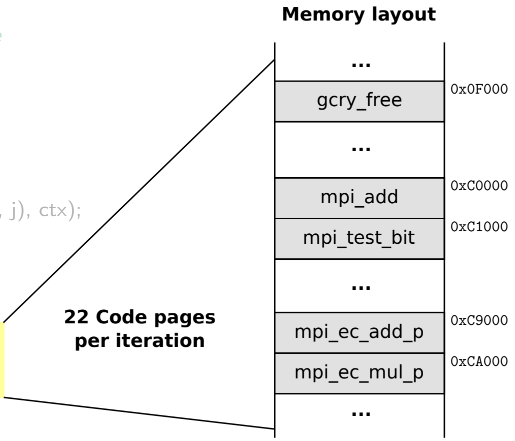

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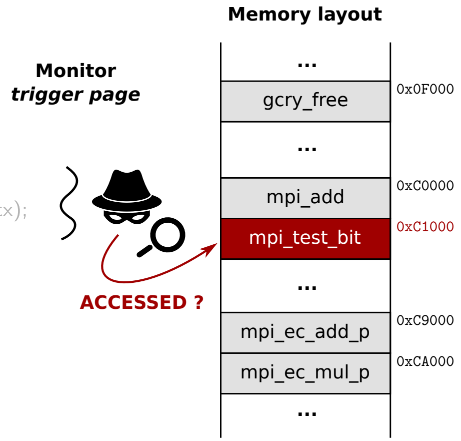

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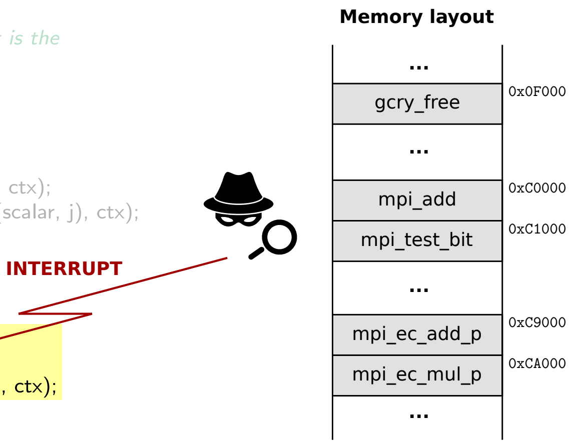

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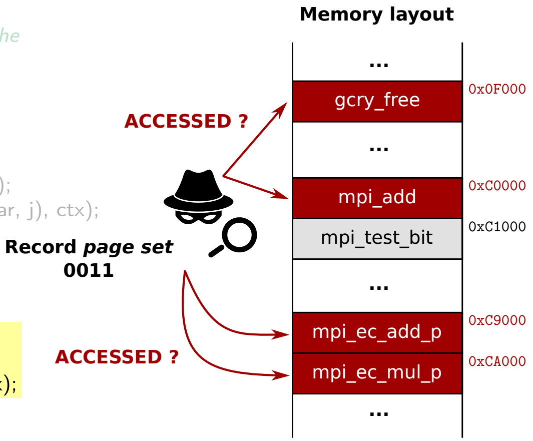

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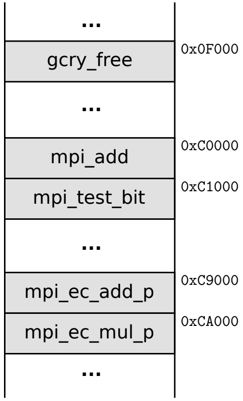
RESUME

Full 512-bit key recovery, single run

Memory layout



Attacking Libgcrypt EdDSA: Cache-Only Channel

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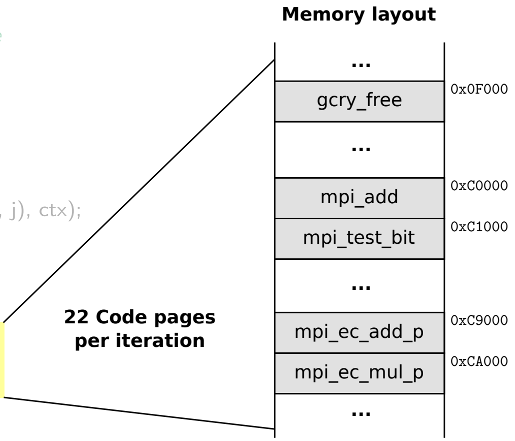

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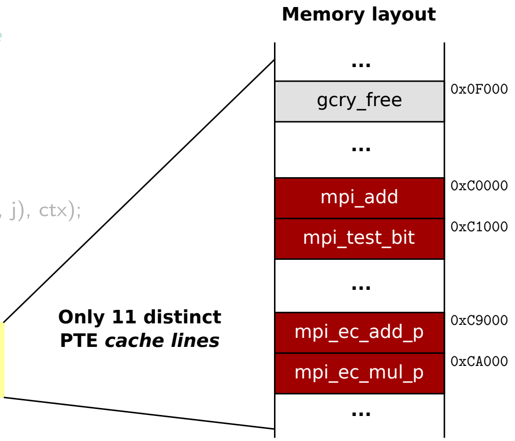

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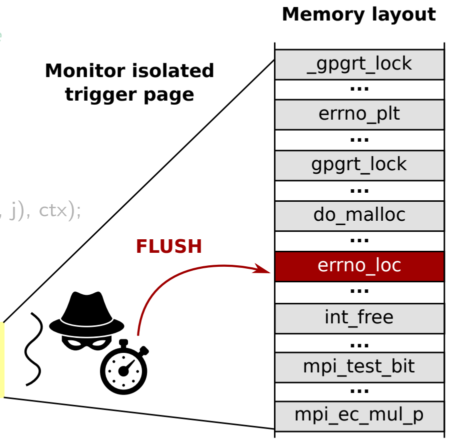

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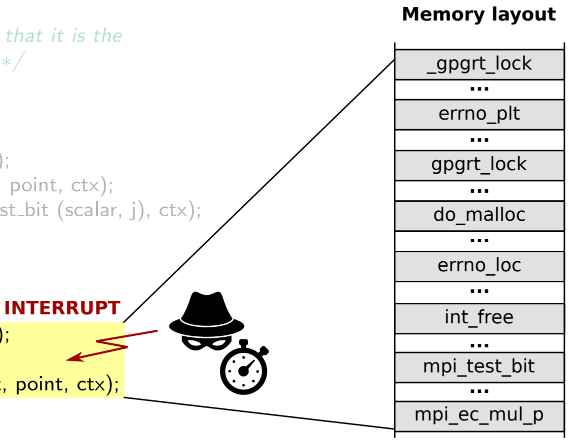

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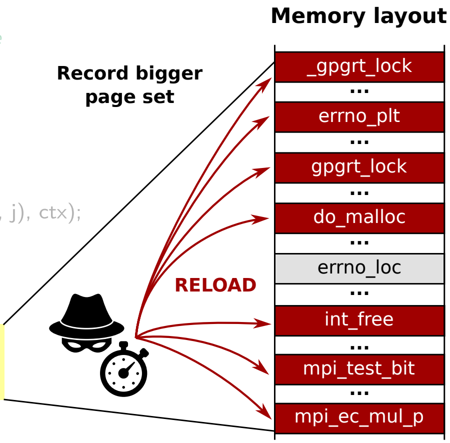

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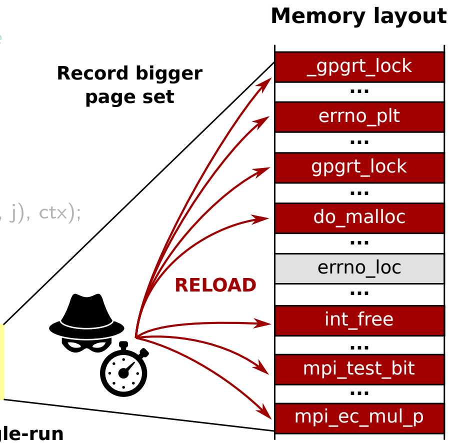
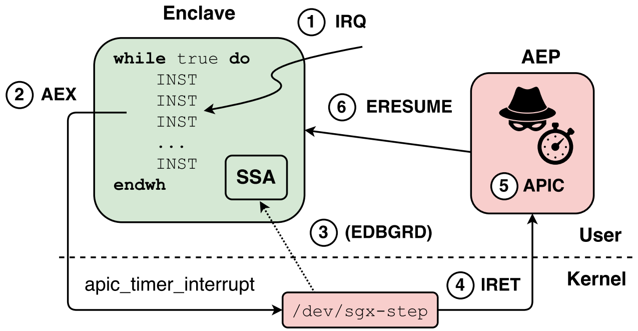


Regex pattern match -> 485/512-bit recovery, single-run

Road Map

SGX-Step: Executing Enclaves One Instruction at a Time

User space APIC timer configuration and page table tracking:



Van Bulck et al. “SGX-Step: A Practical Attack Framework for Precise Enclave Execution Control”, SysTEX 2017 [VBPS17]

SGX-Step: Increasing the Resolution of Page Table Attacks

`strlen` loop

Note: page fault-driven attacks cannot make progress

```
size_t strlen (char *str)
{
  char *s;

  for (s = str; *s; ++s);
  return (s - str);
}
```

Van Bulck et al. "SGX-Step: A Practical Attack Framework for Precise Enclave Execution Control", SysTEX 2017 [VBPS17]

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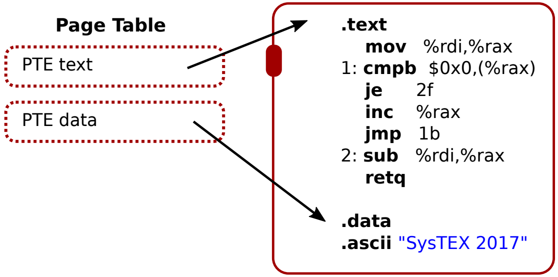

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.text
    mov   %rdi,%rax
1:  cmpb  $0x0,(%rax)
    je    2f
    inc   %rax
    jmp   1b
2:  sub   %rdi,%rax
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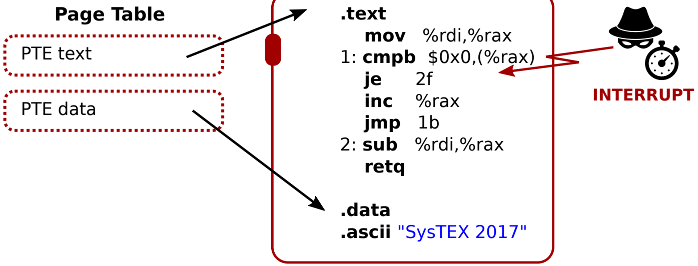

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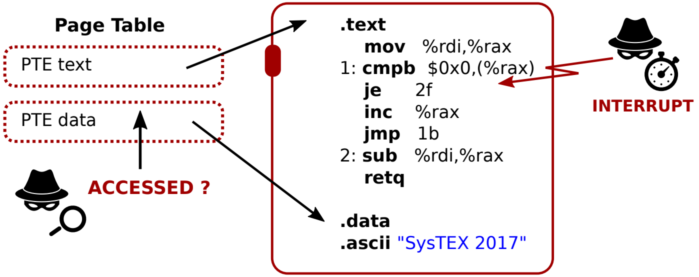

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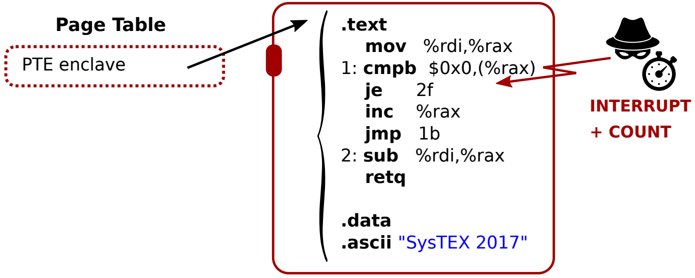
SGX-Step: Increasing the Resolution of Page Table Attacks

Intel SGX Developer Guide [Int17]

"aligning specific code and data blocks to exist entirely within a single page"



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Road Map

Conclusion

Take-Away Message

Enclave memory accesses can be learned *without* triggering page faults.

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⇒ Do not focus on attack **side-effects** (faults, frequent enclave preemptions)

Conclusion

Take-Away Message

Enclave memory accesses can be learned *without* triggering page faults.

⇒ Do not focus on attack **side-effects** (faults, frequent enclave preemptions)

⇒ Address **root causes of information leakage:**

- Unprotected page table memory (Sanctum [CLD16])
- Secret-dependent control flow/data access (Libgcrypt patch)

Thank you! Questions?

`https://github.com/jovanbulck/sgx-pte`

References I

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T-SGX: Eradicating Controlled-Channel Attacks Against Enclave Programs.
In *24th Annual Network and Distributed System Security Symposium (NDSS)*, 2017.

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J. Van Bulck, F. Piessens, and R. Strackx.
SGX-Step: A practical attack framework for precise enclave execution control.
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J. Van Bulck, N. Weichbrodt, R. Kapitza, F. Piessens, and R. Strackx.
Telling your secrets without page faults: Stealthy page table-based attacks on enclaved execution.
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Y. Xu, W. Cui, and M. Peinado.
Controlled-channel attacks: Deterministic side channels for untrusted operating systems.
In *2015 IEEE Symposium on Security and Privacy*, pp. 640–656. IEEE, 2015.

IPI Latency Microbenchmarks

Table: IPI latency in terms of the number of instructions executed by the victim after accessing the trigger page.

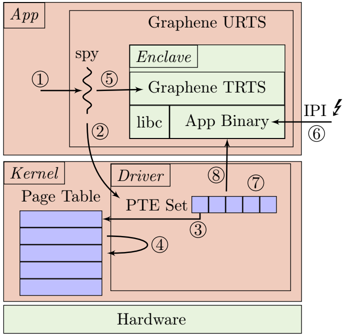
	ACCESSED		FLUSH+FLUSH		
Experiment	**Mean**	σ	**Mean**	σ	**Zero %**
`nop`	431.70	34.11	0.65	17.65	99.84
add register	176.30	14.60	0.15	6.18	99.94
add memory	32.45	2.79	0.06	1.92	99.88
`nop` nocache	0.02	0.39	–	–	–

Putting it All Together: Inferring Page Access Patterns

Re-usable attack framework: Graphene-SGX [TPV17]

- Explicitly monitor **trigger page(s)**
- Capture max info in **page sets** $\leftrightarrow$ #PF-sequences
- Offline analysis: extract **access patterns**

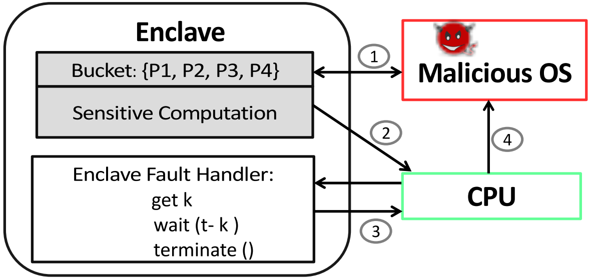
$\Rightarrow$ overcome measurement *noise*/ *latency*/ *granularity*



Proposed Solutions: Hiding Enclave Page Faults

Contractual execution (prototype hardware): [SCNS16]

1. Inform memory requirements
2. Page fault = contract violation
3. CPU delivers fault directly to enclave

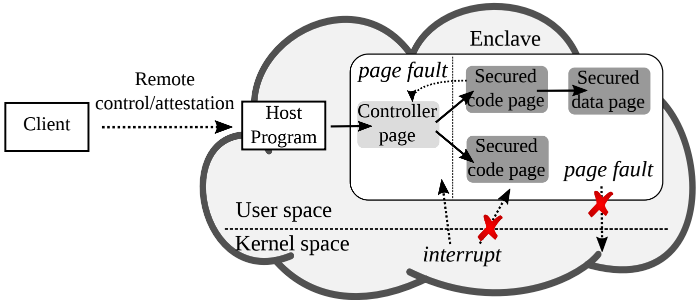


Shinde et al. "Preventing page faults from telling your secrets", AsiaCCS 2016. [SCNS16]

Proposed Solutions: Hiding Enclave Page Faults

T-SGX (Intel x86 compatible): [SLKP17]

1. Wrap enclave code in TSX transactions
2. In-enclave transaction abort handler for page faults



Shih et al. "T-SGX: Eradicating controlled-channel attacks against enclave programs", NDSS 2017. [SLKP17]