

Towards Availability and Real-Time Guarantees for Protected Module Architectures

Jo Van Bulck, Job Noorman, Jan Tobias Mühlberg and Frank Piessens

March 14, 2016

“Embedded-systems security is, for lack of a better word, a mess.”

– John Viega & Hugh Thompson

VIEGA John, THOMPSON Hugh, *The state of embedded-device security (spoiler alert: It's bad)*, IEEE Security & Privacy (10.5), September 2012, pp. 68-70.

Motivation: Embedded Systems Security

Embedded

- Low-cost, low-power
- Mixed-criticality context

=> *Single-address-space*



Conventional

- Resource-intensive
- General-purpose

=> MMU/MPU

=> Kernel mode

<> *TCB reduction*

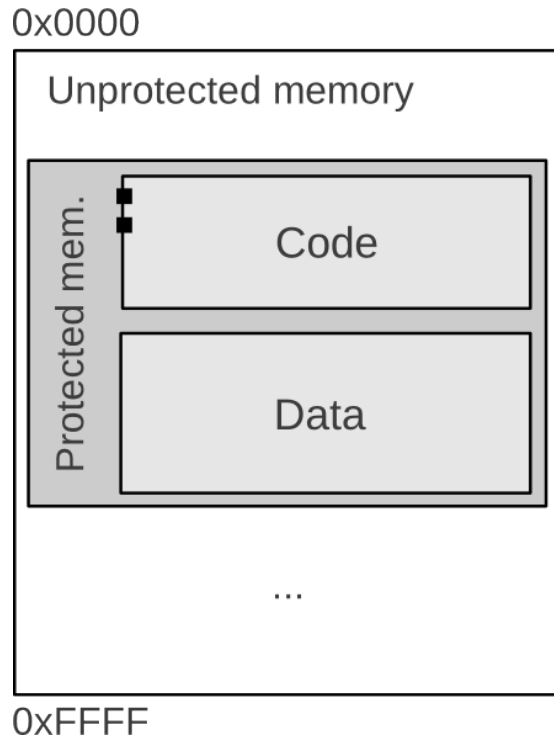
KOEBERL, Patrick, et al. *Trustlite: A security architecture for tiny embedded devices*. EuroSys. ACM (2014).

MCKEEN, Frank, et al. *Innovative instructions and software model for isolated execution*. HASP@ ISCA. 2013.

Roadmap

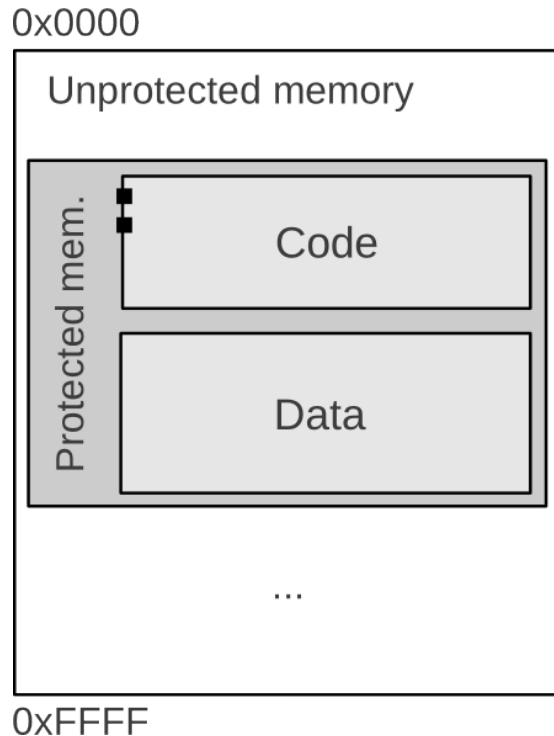
1. Protected Module Architectures
2. Research Objectives
3. Interruptible Isolated Execution
4. Secure Multithreading
5. Conclusion

Protected Module Architectures



- **Isolated execution** areas in a single-address-space

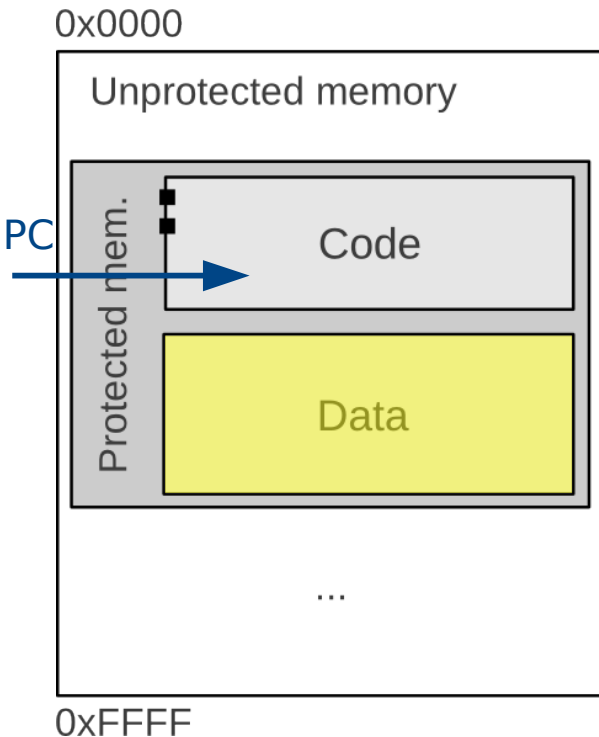
Protected Module Architectures



- **Isolated execution** areas in a single-address-space
- **Program counter** based access control mechanism

From \ to	Protected			Unprotected
	Entry	Code	Data	
Protected	r-x	r-x	rw-	rwX
Unprotected / other SPM	r-x	r--	---	rwX

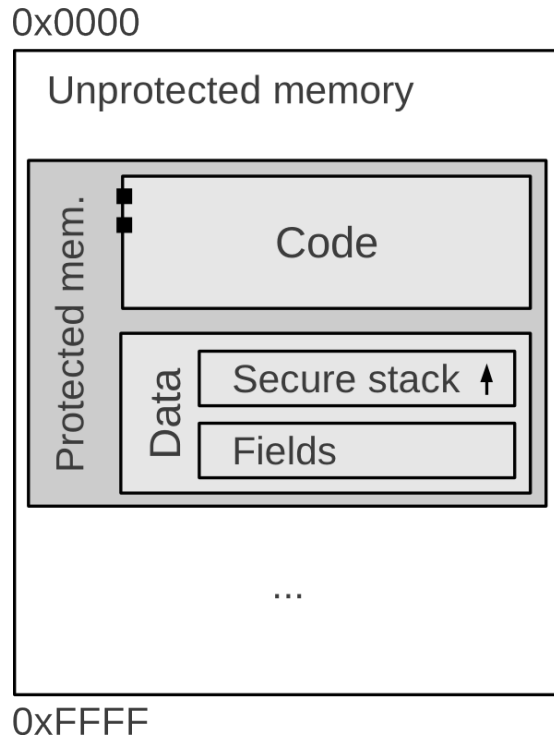
Protected Module Architectures



- **Isolated execution** areas in a single-address-space
- **Program counter** based access control mechanism

From \ to	Protected			Unprotected
	Entry	Code	Data	
Protected	r-x	r-x	rw-	rwX
Unprotected / other SPM	r-x	r--	---	rwX

Protected Module Architectures



- **Isolated execution** areas in a single-address-space
- **Program counter** based access control mechanism
- Secure fully abstract **compilation**

From \ to	Protected			Unprotected
	Entry	Code	Data	
Protected	r-x	r-x	rw-	rwX
Unprotected / other SPM	r-x	r--	---	rwX

Sancus PMA

- **Zero-software TCB**

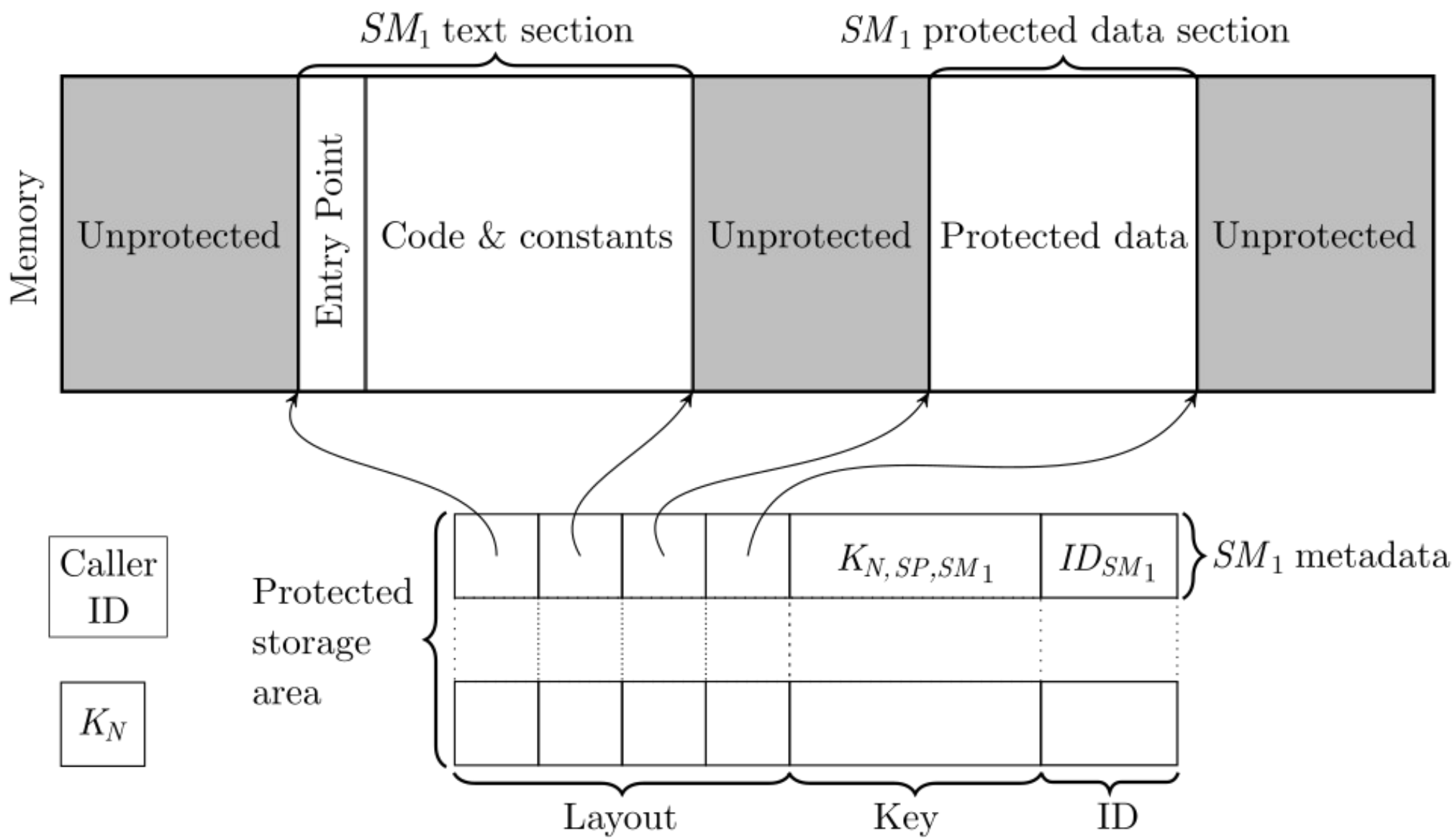
→ extended openMSP430 instruction set

Sancus PMA

- **Zero-software TCB**
 - extended openMSP430 instruction set
- SM == unit of **isolation + authentication**
 - *remote attestation / secure linking*
 - hardware cryptographic key and ID per SM

Sancus PMA

- **Zero-software TCB**
 - extended openMSP430 instruction set
- SM == unit of **isolation + authentication**
 - *remote attestation / secure linking*
 - hardware cryptographic key and ID per SM
- Dedicated secure C **compiler**
 - generates `sm_entry/exit` asm stubs



Contents

1. Protected Module Architectures
2. Research Objectives
3. Interruptible Isolated Execution
4. Secure Multithreading
5. Conclusion

Research Objectives

PMAAs assume the presence of an attacker:

- ☺ HW-enforced SM **confidentiality / integrity**
- ☹ no **availability guarantees**

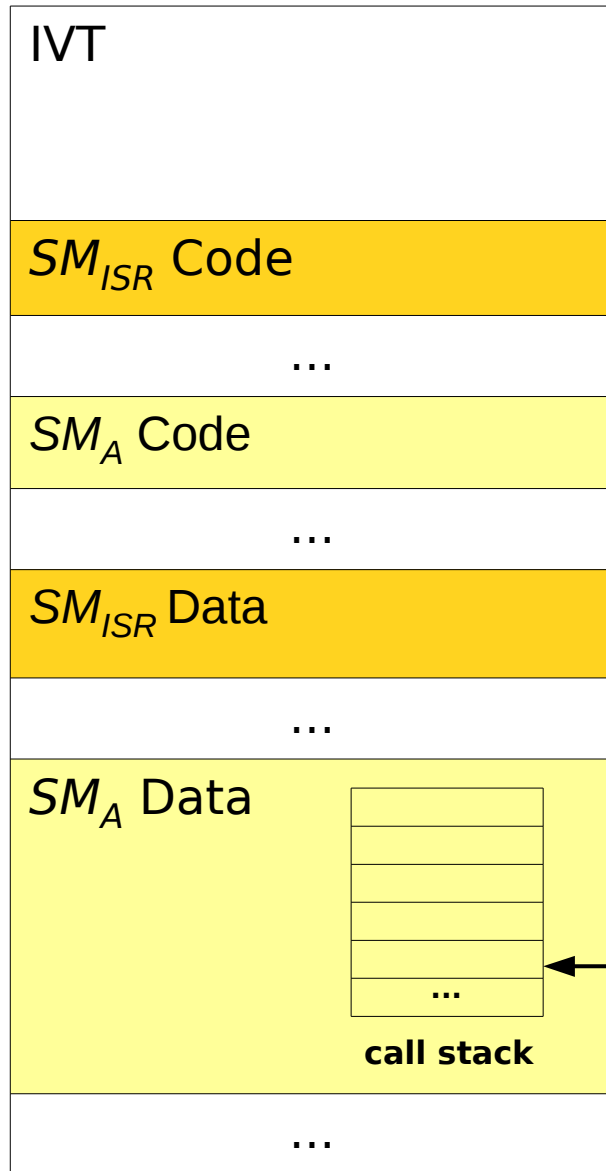
=> concurrent execution of *isolated threads* via an *unprivileged* preemptive scheduler

Contents

1. Protected Module Architectures
2. Research Objectives
3. Interruptible Isolated Execution
4. Secure Multithreading
5. Conclusion

Interruptible and Reentrant SMs

Memory



Register File

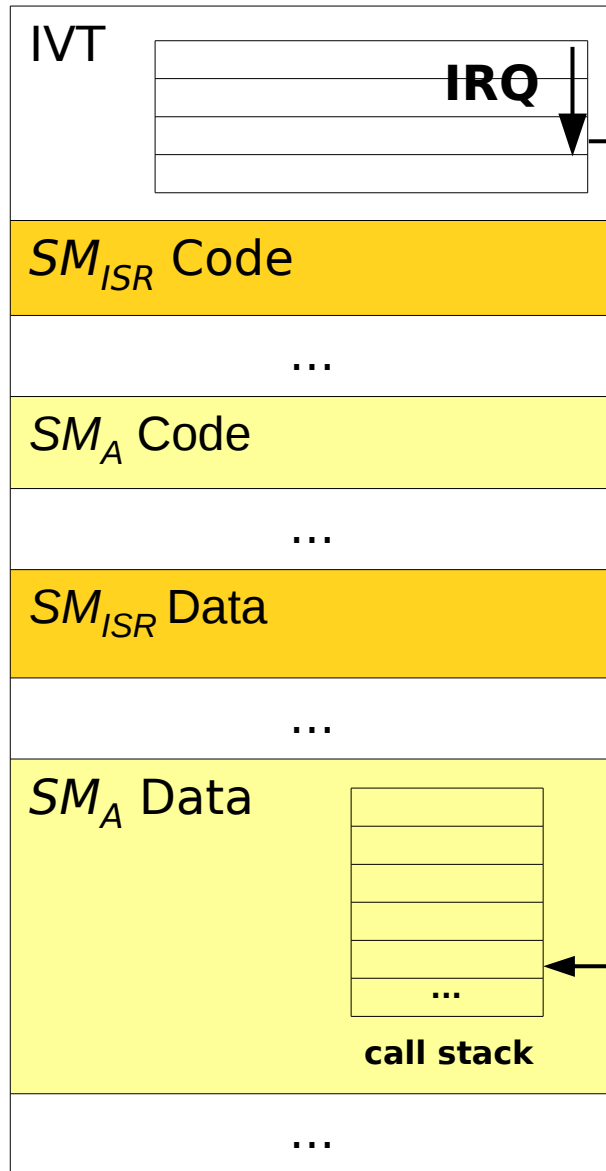
R0 = PC
R1 = SP
R2 = SR
R3 = cst
R4 = general
...
R15 = general

Current SM = SM_A

Previous SM = x

Interruptible and Reentrant SMs

Memory



Register File

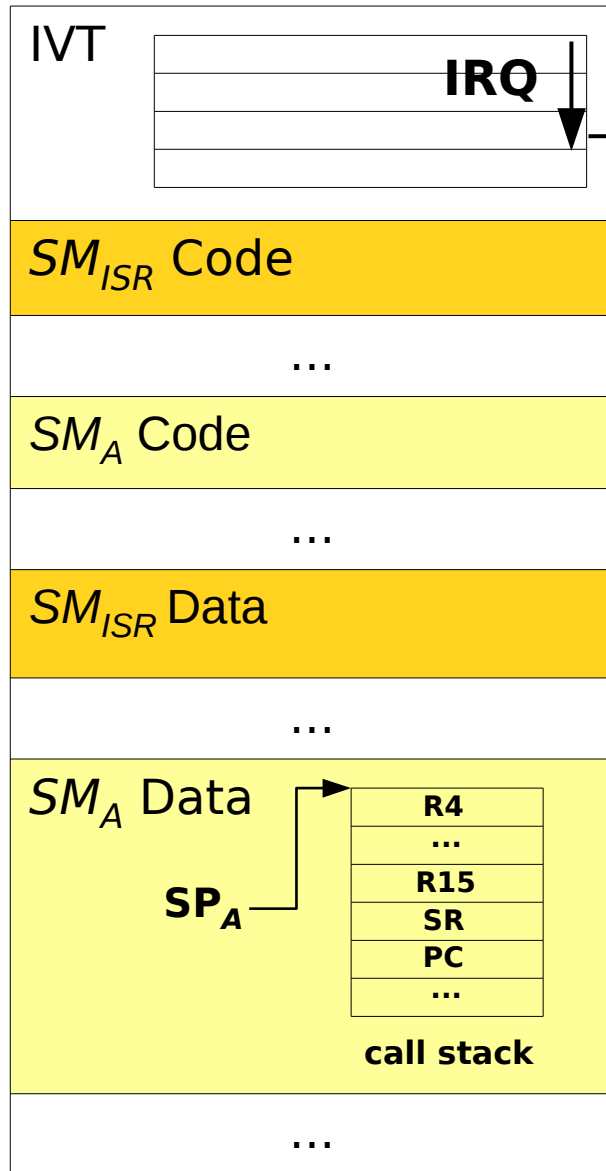
R0 = PC
R1 = SP
R2 = SR
R3 = cst
R4 = general
...
R15 = general

Current SM = SM_A

Previous SM = x

Interruptible and Reentrant SMs

Memory



Register File

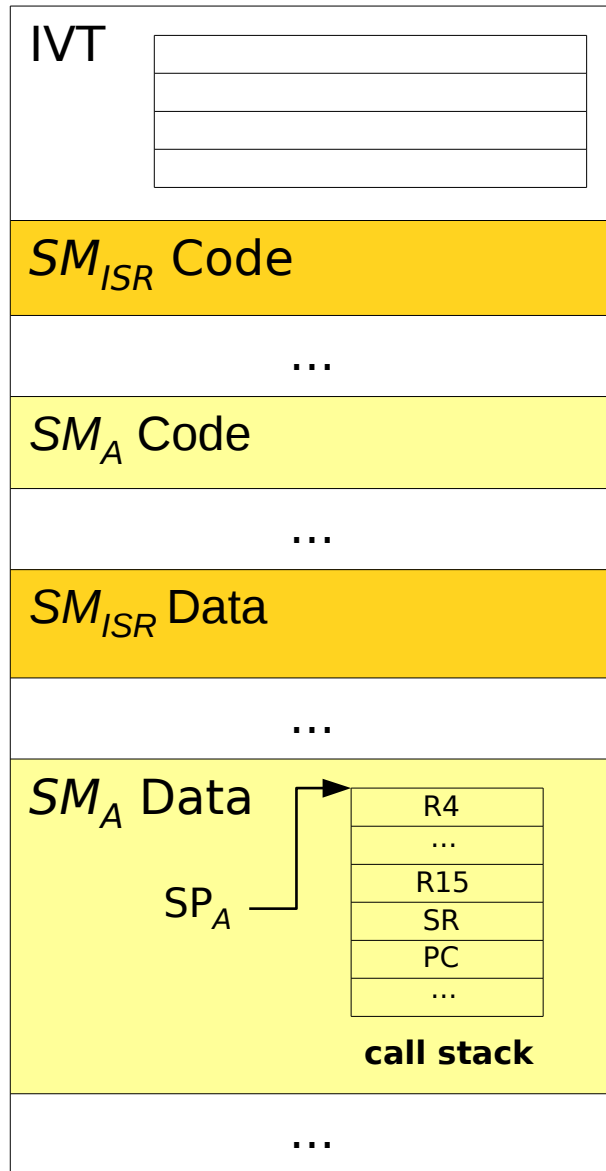
R0 = PC
R1 = 0x0
R2 = 0x0
R3 = cst
R4 = 0x0
...
R15 = 0x0

Current SM = SM_A

Previous SM = x

Interruptible and Reentrant SMs

Memory



sm_entry.s

Register File

R0 = PC
R1 = 0x0
R2 = 0x0
R3 = cst
R4 = 0x0
...
R15 = 0x0

Current SM = SM_{ISR}

Previous SM = IRQ

Discussion / Future Work

=> *Zero-software TCB for SM conf / int*

- **Atomicity** constraints (secure compilation)
 - deterministic *interrupt latency*
 - *TOCTOU*: callee authentication
 - *sm_entry*: restore SP, caller authentication

Discussion / Future Work

=> *Zero-software TCB for SM conf / int*

- **Atomicity** constraints (secure compilation)
 - deterministic *interrupt latency*
 - *TOCTOU*: callee authentication
 - *sm_entry*: restore SP, caller authentication
- **Untrusted ISRs**: integrity of `reti` flow

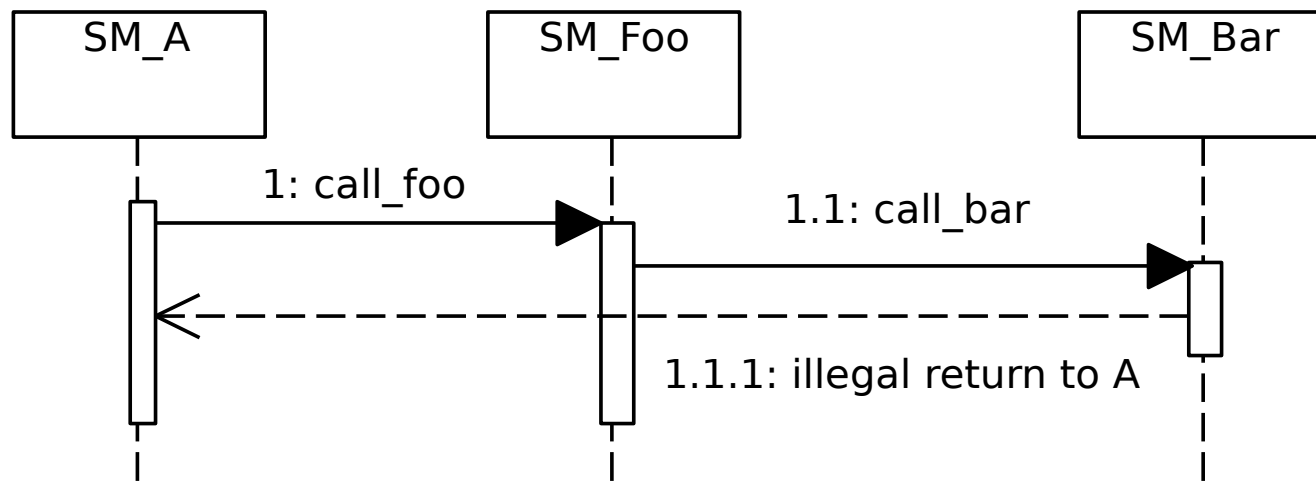
Contents

1. Protected Module Architectures
2. Research Objectives
3. Interruptible Isolated Execution
4. Secure Multithreading
5. Conclusion

Traditional Multithreading vs. PMA

Synchronous control flow in address space

- unit of **threading** >> **SM**
- inter-SM call/return **integrity**
- compiler-generated `sm_entry` stubs



Protected FreeRTOS Scheduler

- **Interleaved** execution of multiple threads
 - cooperative prototype: `yield()`

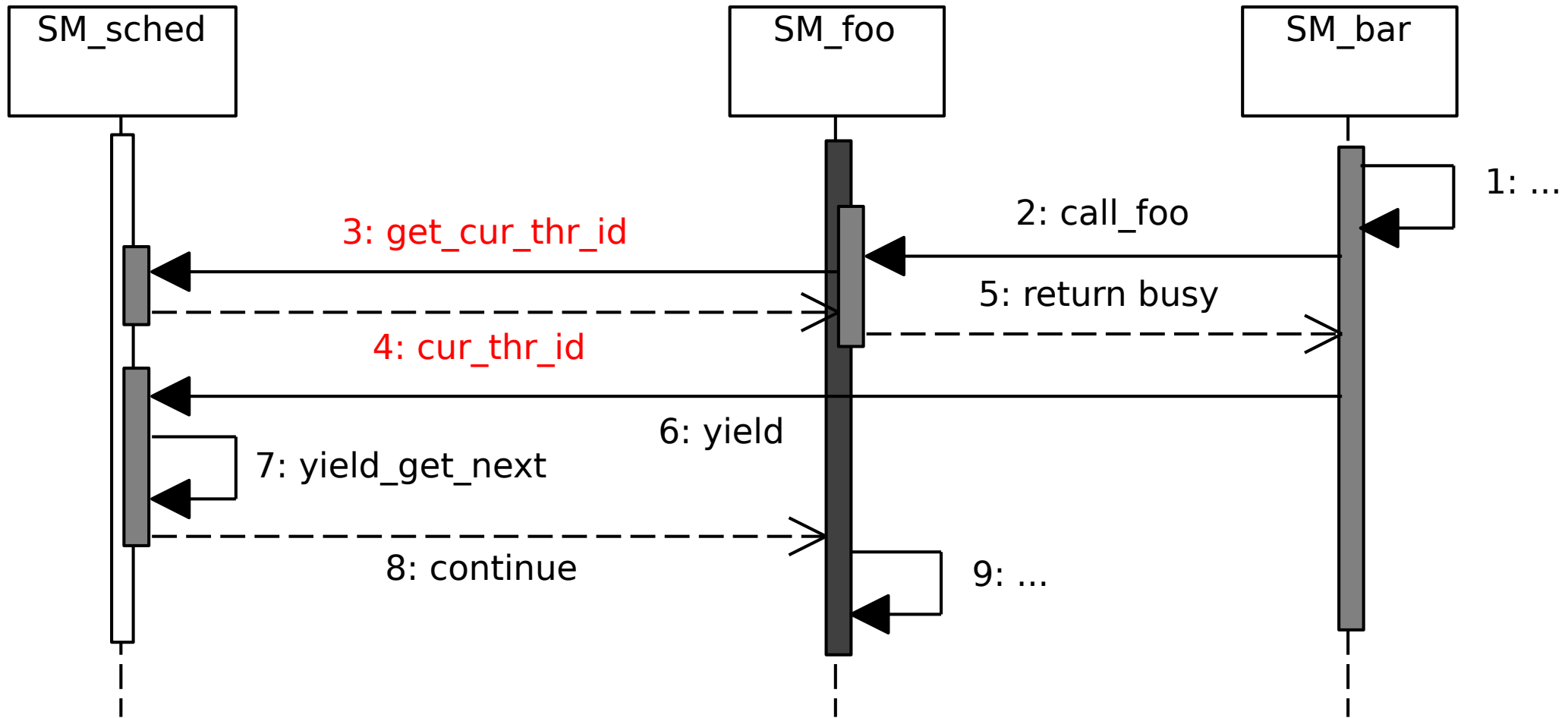
Protected FreeRTOS Scheduler

- **Interleaved** execution of multiple threads
 - cooperative prototype: `yield()`
- **Unprivileged**: scheduling decision only
 - store “*return address*” to continue thread
 - protected scheduler state

Protected FreeRTOS Scheduler

- **Interleaved** execution of multiple threads
 - cooperative prototype: `yield()`
- **Unprivileged**: scheduling decision only
 - store “*return address*” to continue thread
 - protected scheduler state
- Secure **linking**: `sm_entry` violation report

Threading-aware SMs



Discussion / Future Work

=> *Isolated cross-SM control flow threads*

{ Scheduling **policy encapsulation**
SMs guard internal **consistency**

Discussion / Future Work

=> *Isolated cross-SM control flow threads*

{ Scheduling **policy encapsulation**
SMs guard internal **consistency**

Future work:

- preemptive FreeRTOS
- SM-internal multithreading
- asynchronous inter-thread communication

Contents

1. Protected Module Architectures
2. Research Objectives
3. Interruptible Isolated Execution
4. Secure Multithreading
5. Conclusion

Conclusion

=> Strong availability (real-time) guarantees on a partially compromised platform

- Confined and explicit **TCB**
 - HW-only for SM conf / int
 - SW layer: *principle of least privilege*
- Secure **compilation** in preemptive context

Towards Availability and Real-Time Guarantees for Protected Module Architectures

Jo Van Bulck, Job Noorman, Jan Tobias Mühlberg and Frank Piessens

<https://distrinet.cs.kuleuven.be/software/sancus/>